

DDR4 Memory Model

Overview

Memory is a major part of every electronic product. Every system on chip (SoC) contains embedded memories and must also interface with external memory components. The operation of these interfaces impacts both SoC functionality and performance, making memory interface verification a crucial step in the SoC development process.

Cadence® Memory Models are the gold standard for memory interface verification. Used by more than 500 customers, Cadence Memory Models provide support for 6,500 memories spanning 60 memory interface types and 85 memory manufacturers.



Vendor Certification

Memory models for commercial memory components are based on the manufacturer's datasheets and are then provided to the manufacturer for certification. This closed-loop quality control process means that you can trust your simulation results. Models for new external memory standards that do not yet have commercial component providers and models for internal memory standards are based upon the specifications provided by the controlling standards body, such as JEDEC, ONFI, and SD Association. Cadence works closely with our early-adopter customers to ensure the quality of these models.

Accurate Timing Analysis

When memory models represent actual memory chips and modules, the memory models include full timing parameters that support accurate gate-level simulations. Timing specs are conveniently displayed in the PureView tool and can be overridden for what-if analysis.

Second Source Evaluation

Memory models are inserted into a testbench as generic models that are then associated with a personality file to represent a specific component. This makes it easy to do second-source evaluation of memory components.

Specification Support

DDR4SDRAM Memory Model VIP supports the officially released JESD79-4 Rev 1.0 Specification and 3DS extensions.

Key Features

- The UVM agent contains model configuration information directly and natively, along with providing a UVM API for configuring and accessing that configuration.
- ememory SOMAs are auto translated to a UVM config class equivalent, so the agent's cfg contains the SOMA information natively in UVM SV.
- The API, for example, includes a simple method for doing the equivalents of somaset / somaload.
- Supports command decoding.
- Supports 3DS Read/Write commands for 2H/4H/8H combinations
- Precharge, Activate, Read, Write, Mode Register Write, Write levelling, ODT checks, Power Down, Self Refresh, Initializations and all related timing checks.
- A16..A14 are multiplexed with ras, cas and weabar pins and dedicated act pin for Activate command.
- Data Width, Density: 4, 8 and 16. 2Gb to 16Gb
- New mode registers and associated settings.
- Speed: 1600, 1866, 2133
- Modeling the concept and the timing associated with the back-to-back accesses to the same and difference bank group.
- More MPR registers organized as pages. More options of reading those registers and preamble training.
- Some important setting of the more registers are shadowed into page-2 MPRs.
- Data on the bus can be inverted during both read and write to save power. Both Data Mask and Data Bus inversion features can be set through mode registers.
- Allows mode registers of each DRAM on the DIMM to be programmed independently.
- Allows CSBAR to be asserted a few cycles before actual command details.
- CRC is checked for writes and error is flagged to the controller. CRC failures will let the write go through in the case that Data Mask is disabled and will block the writes in the case that Mask is enabled.
- Parity checking is off by default, but when enabled parity is checked for each command before execution and also detailed recovery in case of errors and reporting of logs through MPR Reads.
- Allows the DRAM to operate in 2N mode.
- tDQSK jitters are officially defined in the spec and they drift per operating voltage and temperature. The VIP models this and allows the controller to configure the drift and skew.
- Allows both 1CK and 2CK preambles to be selected for both read and writes.
- Normal mode refresh, Self refresh, Temperature controller self refresh, Low Power Array self refresh, and Fine-granularity refresh
- Preserving the mode registers setting, but data is lost.
- Complete modelling of all RTT values, RTT_NOM/RTT_Park/RTT_Wr with the internal register representing the value of RTT at a given point of time, based on the mode of operation.



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