DDR3 Memory Model

Overview

Memory is a major part of every electronic product. Every system on chip (SoC) contains embedded memories and must also interface with external memory components. The operation of these interfaces impacts both SoC functionality and performance, making memory interface verification a crucial step in the SoC development process.

Cadence® Memory Models are the gold standard for memory interface verification. Used by more than 500 customers, Cadence Memory Models provide support for 6,500 memories spanning 60 memory interface types and 85 memory manufacturers.

Vendor Certification

 Memory models for commercial memory components are based on the manufacturer's datasheets and are then provided to the manufacturer for certification. This closed-loop quality control process means that you can trust your simulation results. Models for new external memory standards that do not yet have commercial component providers and models for internal memory standards are based upon the specifications provided by the controlling standards body, such as JEDEC, ONFi, and SD Association. Cadence works closely with our early-adopter customers to ensure the quality of these models.

Accurate Timing Analysis

When memory models represent actual memory chips and modules, the memory models include full timing parameters that support accurate gate-level simulations. Timing specs are conveniently displayed in the PureView tool and can be overridden for what-if analysis.

Second Source Evaluation

Memory models are inserted into a testbench as generic models that are then associated with a personality file to represent a specific component. This makes it easy to do second-source evaluation of memory components.

Specification Support

The DDR3 SDRAM Memory Model VIP supports the officially released JESD79-3 version of the DDR3 SDRAM specification. The model also supports the 3F version of the specification.

Key Features

- Pre-charge, Activate, Read, Write, Mode Register Write, Write leveling, ODT checks, Power Down, Self Refresh, Initializations and all related timing checks.

- Implements and exposes DDR3SDRAM state machines natively to user's HVL (eg init state, bank state, model state) and performs specified timing checks.

- Data Width, Density: 500M - 8g density, x4 - x16 width

- Speed: 800, 1066, 1333, 1600

- Modeling the concept and the timing associated with the back-to-back accesses to the same and difference bank group

- Multi-purpose register mode with pattern feedback for reads for read level training

- tDQSCK jitter drift per operating voltage and temperature defined in the DDR4 spec can be enabled so the VIP models this according to configured drift and skew

- Normal mode refresh, including refresh rate check, Self Refresh, Partial Array Self Refresh, Extended Temperature self refresh

- Model tracking state changes and assertion check and timing adjustments throughout the change sequence steps

- All mode register fields configurations

- Vendors: Micron, Elpida, Eorex, Hynix, Naya, Samsung, Windbond

- Leveling checks and feedback response including option for bit-to-bit skew

- Data on the bus for writes is appropriately masked according to mode enabled and dm bus state