VIP Datasheet

# Accelerated VIP for SIMCARD

## Overview

Sometimes chips are just too big to verify with logic simulation software. SoCs comprised of tens of millions of logic gates will bog down software simulators, even when running on the fastest servers.

Simulating big designs requires hardware-assisted verification, an approach that uses special-purpose hardware, like Cadence® Palladium® XP systems, to dramatically boost simulation performance.

Cadence Accelerated VIPs are complementary products to Cadence simulation VIP and SpeedBridges. Accelerated VIPs are used to funnel data to the user's design-under-test and respond to stimulus received from it. Monitor functions such as collecting coverage and setting callbacks are not included.

Tuned for performance, AVIPs are an integral component in a simulation acceleration environment, speeding up verification 10's to 1,000's of times relative to simulation. The level of acceleration gain is dependent on the user's individual testbench and DUT synchronizations.

## Specification Support

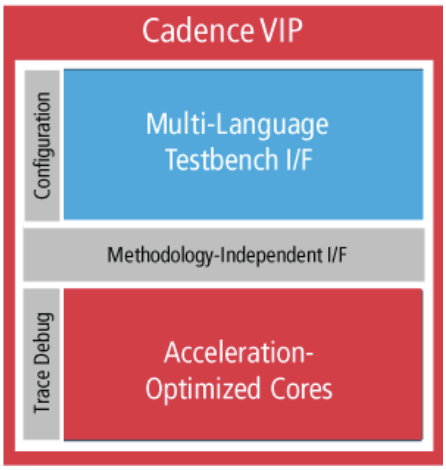
The SimCard AVIP is based on the SIM BFM Requirement Specification, Version 0.7 –14 August 2012.

## Usage Options

- ☐ Simulation Acceleration
- ☑ HW/SW Co-Verification

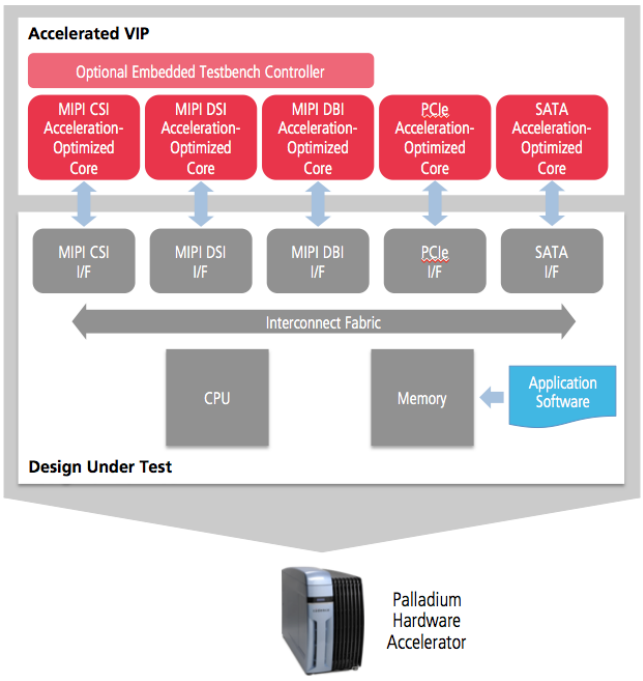
## Supported Design-Under-Test Configurations

| | | |
|---|---|---|
| ☑ Host | ☐ Device | ☐ Port Multiplier |
| ☑ Full Stack | ☐ Controller-only | ☐ PHY-only |




## Product Highlights

- Synthesizable Bus Functional Model (BFM) compliant with ISO/IES 7816-3 standard that supports Card mode only (Slave)
- Internal registers for configuration
- Configurable T0/T1 protocol parameters
- Support direct/inverse mode data convention
- Supports complete activation/deactivation sequence
- Integrated card state monitor register
- Error injection for sent packets and error detection for received packets
- HW/SW co-verification mode, which supports:
  - –Descriptor-based programming model
  - –Scalable internal memory for program and local data
  - –AHB Slave interface providing full register access and internal memory access
  - –DMA and DMA Scatter-Gather capabilities via AHB Master interface
  - –Incremental and pseudo-random data generation
  - –Configurable H/W and S/W start/stop conditions
  - –IRQ with maskable interrupt status registers




## HW/SW Co-Verification

With the HW/SW co-verification approach, both the test environment and the design under test run in the Palladium XP system. This results in huge performance gains – typically 10,000X to 100,000X faster than logic simulation. That kind of speed enables the verification of software along with the hardware design. This enables hardware/software integration bugs to be efficiently discovered and fixed – a task that would be nearly impossible to manage otherwise. To facilitate the HW/SW co-verification approach, application software is often used to run tests and monitor results.

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