

Accelerated VIP for SATA 1.5G/3G/6G

Overview

Sometimes chips are just too big to verify with logic simulation software. SoCs comprised of tens of millions of logic gates will bog down software simulators, even when running on the fastest servers.

Simulating big designs requires hardware-assisted verification, an approach that uses special-purpose hardware, like Cadence® Palladium® XP systems, to dramatically boost simulation performance.

Cadence Accelerated VIPs are complementary products to Cadence simulation VIP and SpeedBridges. Accelerated VIPs are used to funnel data to the user’s design-under-test and respond to stimulus received from it. Monitor functions such as collecting coverage and setting callbacks are not included.

Tuned for performance, AVIPs are an integral component in a simulation acceleration environment, speeding up verification 10’s to 1,000’s of times relative to simulation. The level of acceleration gain is dependent on the user’s individual testbench and DUT synchronizations.

Specification Support

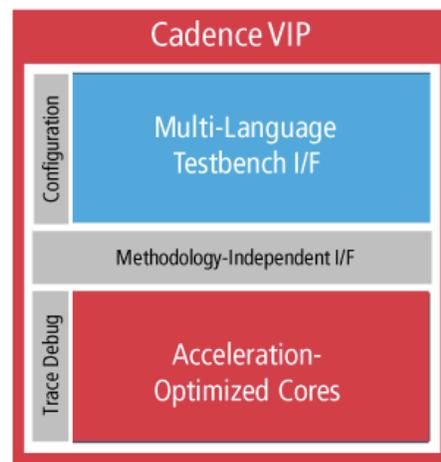
The SATA AVIP is based on the Serial ATA Specification 3.0 and the ATA Command Set specification, ATA8 version.

Usage Options

- Simulation Acceleration
- HW/SW Co-Verification

Supported Design-Under-Test Configurations

- | | | |
|--|--|--|
| <input checked="" type="checkbox"/> Host | <input type="checkbox"/> Device | <input type="checkbox"/> Port Multiplier |
| <input checked="" type="checkbox"/> Full Stack | <input type="checkbox"/> Controller-only | <input type="checkbox"/> PHY-only |

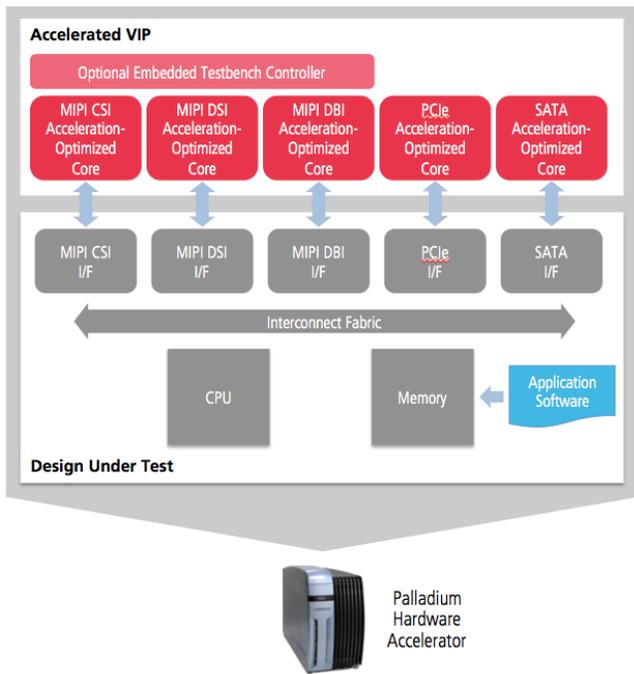


Product Highlights

- Supports the SATA Device for use with simulation acceleration and In-Circuit Emulation. When used with In-Circuit Emulation, it can be used in both STB and LA modes.
- The memory inside the SATA Device can be read and written using the Palladium XP MARG interface, or by using the xeDebug memory commands. This allows a disk image to be loaded and unloaded into the SATA Device as part of a test.
- Supports the Serial-ATA PHY Interface Specification (SAPIS) drafted by Intel Corp
- Supports 10-bit and 20-bit data interfaces
- Supports Gen 1, Gen 2, and Gen 3 speeds

Supports SATA Device Disk for the following classes of ATA commands (ATA-8):

- PIO Read and Write
- DMA Read and Write
- Non-Data Commands
- Queued DMA Commands



HW/SW Co-Verification

With the HW/SW co-verification approach, both the test environment and the design under test run in the Palladium XP system. This results in huge performance gains – typically 10,000X to 100,000X faster than logic simulation. That kind of speed enables the verification of software along with the hardware design. This enables hardware/software integration bugs to be efficiently discovered and fixed – a task that would be nearly impossible to manage otherwise. To facilitate the HW/SW co-verification approach, application software is often used to run tests and monitor results.



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