VIP Datasheet

Accelerated VIP for PCI Express Gen2/Gen3

Overview

Sometimes chips are just too big to verify with logic simulation software. SoCs comprised of tens of millions of logic gates will bog down software simulators, even when running on the fastest servers.

Simulating big designs requires hardware-assisted verification, an approach that uses special-purpose hardware, like Cadence® Palladium® XP systems, to dramatically boost simulation performance.

Cadence Accelerated VIPs are complementary products to Cadence simulation VIP and SpeedBridges. Accelerated VIPs are used to funnel data to the user's design-under-test and respond to stimulus received from it. Monitor functions such as collecting coverage and setting callbacks are not included.

Tuned for performance, AVIPs are an integral component in a simulation acceleration environment, speeding up verification 10's to 1,000's of times relative to simulation. The level of acceleration gain is dependent on the user's individual testbench and DUT synchronizations.

Specification Support

All PCIe transactions are in accordance with the PCI Express 3.0 Specification.

Usage Options

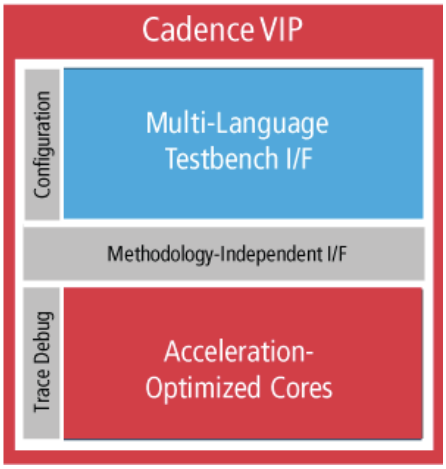
- [x] Simulation Acceleration
- [ ] HW/ SW Co-Verification

Supported Design-Under-Test Configurations

- [x] Root Complex
- [x] End Point
- [ ] Hub/Switch
- [x] Full Stack
- [ ] Controller-only
- [ ] PHY-only

Product Highlights

- 8/16/32-bit PIPE interface
- Serial interface
- Up to 8 lanes
- Power management

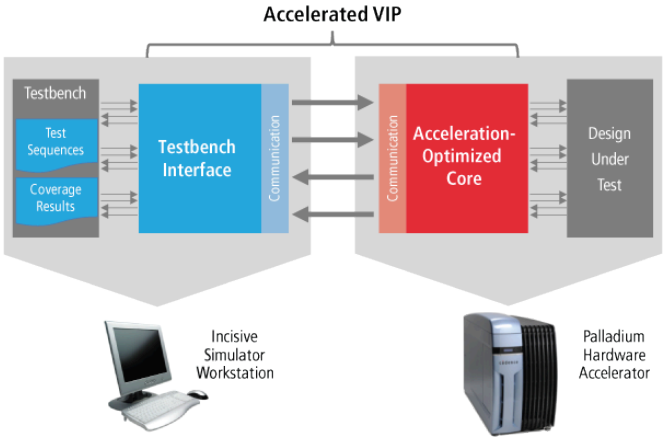


- Complete set of configuration/status registers
- Logs transactions in log file + logging control
- 2.5/5/8 GT/s speeds
- Link equalization
- Backdoor memory access (read/write to own memory)
- Stimulus access to received transactions using callbacks
- Events to control timing of transactions (reduces HW/SW syncs and gives control to stimulus)
- Single root I/O virtualization (SR-IOV)
- Fully supports the following transactions:
  –Memory Read
  –Memory Write
  –Memory Read Lock
  –I/O Read
  –I/O Write
  –Configuration Read (Type 0 and Type 1)
  –Configuration Write (Type 0 and Type 1)
  –Messages with data and without data

Simulation Acceleration

In simulation acceleration, the Cadence Palladium XP system works in conjunction with the Cadence Incisive® Simulator to divide up the simulation task. The Palladium XP runs the design under test while the Incisive simulator runs the testbench. Accelerated VIP is inserted for each of the standard interfaces in the design with the testbench interface running on Incisive and the acceleration-optimized core running on the Palladium XP.

Most of the testbench components employed in simulation can be reused, which saves set-up time and preserves the controllability and observeability of traditional logic simulation. With this approach, performance is often up to 1000X faster than logic simulation.



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