

Accelerated VIP for MIPI CSI-2

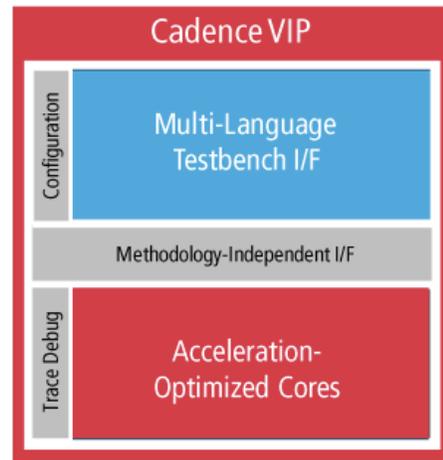
Overview

Sometimes chips are just too big to verify with logic simulation software. SoCs comprised of tens of millions of logic gates will bog down software simulators, even when running on the fastest servers.

Simulating big designs requires hardware-assisted verification, an approach that uses special-purpose hardware, like Cadence® Palladium® XP systems, to dramatically boost simulation performance.

Cadence Accelerated VIPs are complementary products to Cadence simulation VIP and SpeedBridges. Accelerated VIPs are used to funnel data to the user’s design-under-test and respond to stimulus received from it. Monitor functions such as collecting coverage and setting callbacks are not included.

Tuned for performance, AVIPs are an integral component in a simulation acceleration environment, speeding up verification 10’s to 1,000’s of times relative to simulation. The level of acceleration gain is dependent on the user’s individual testbench and DUT synchronizations.



Specification Support

This VIP supports specification versions:

- MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2), Version 1.01.00 Revision 0.04
- CSI-2 BFM Requirement Specification, Version 0.10

Usage Options

- Simulation Acceleration
- HW/SW Co-Verification

Supported Design-Under-Test Configurations

- | | | |
|--|--|-------------------------------------|
| <input checked="" type="checkbox"/> Host | <input checked="" type="checkbox"/> Peripheral | <input type="checkbox"/> Hub/Switch |
| <input checked="" type="checkbox"/> Full Stack | <input type="checkbox"/> Controller-only | <input type="checkbox"/> PHY-only |

Product Highlights

- Synthesizable Bus Functional Model (BFM) compliant with CSI-2 standard
- Internal registers for configuration
- Configurable to CSI-2 Peripheral or CSI-2 Host
- Fully configurable CSI-2 packets in Peripheral mode
- Embedded digital model of D-PHY
- Error injection in Peripheral mode and error detection in Host mode – supporting CSI-2 level (ECC, CRC) protocol error detection

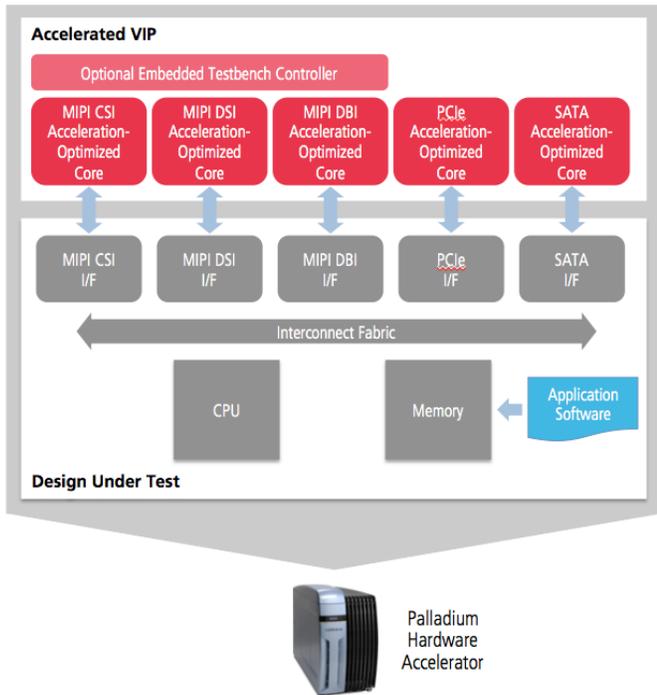
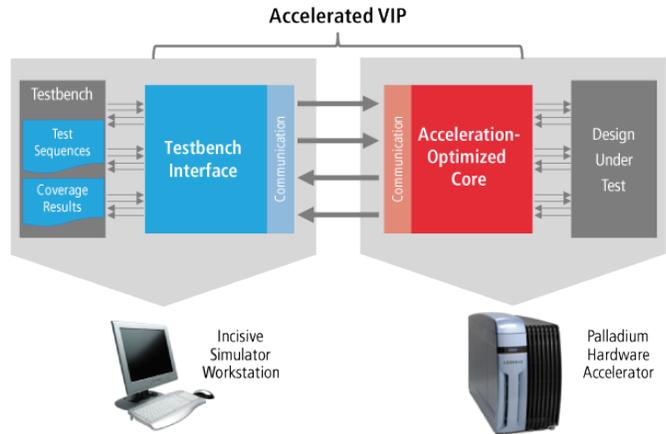
HW/SW co-verification mode, which supports:

- Descriptor-based programming model
- Scalable internal memory for program and local data
- AHB Slave interface providing full register access and internal memory access
- DMA and DMA Scatter-Gather capabilities via AHB Master interface
- Incremental and pseudo-random data generation
- Configurable H/W and S/W start/stop conditions
- Support for simple and embedded programming loops
- IRQ with maskable interrupt status registers

Simulation Acceleration

In simulation acceleration, the Cadence Palladium XP system works in conjunction with the Cadence Incisive® Simulator to divide up the simulation task. The Palladium XP runs the design under test while the Incisive simulator runs the testbench. Accelerated VIP is inserted for each of the standard interfaces in the design with the testbench interface running on Incisive and the acceleration-optimized core running on the Palladium XP.

Most of the testbench components employed in simulation can be reused, which saves set-up time and preserves the controllability and observability of traditional logic simulation. With this approach, performance is often up to 1000X faster than logic simulation.



HW/SW Co-Verification

With the HW/SW co-verification approach, both the test environment and the design under test run in the Palladium XP system. This results in huge performance gains – typically 10,000X to 100,000X faster than logic simulation. That kind of speed enables the verification of software along with the hardware design. This enables hardware/software integration bugs to be efficiently discovered and fixed – a task that would be nearly impossible to manage otherwise. To facilitate the HW/SW co-verification approach, application software is often used to run tests and monitor results.



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