

Accelerated VIP for HDMI 1.4

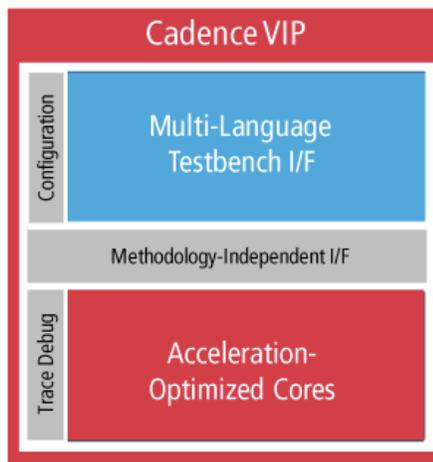
Overview

Sometimes chips are just too big to verify with logic simulation software. SoCs comprised of tens of millions of logic gates will bog down software simulators, even when running on the fastest servers.

Simulating big designs requires hardware-assisted verification, an approach that uses special-purpose hardware, like Cadence® Palladium® XP systems, to dramatically boost simulation performance.

Cadence Accelerated VIPs are complementary products to Cadence simulation VIP and SpeedBridges. Accelerated VIPs are used to funnel data to the user’s design-under-test and respond to stimulus received from it. Monitor functions such as collecting coverage and setting callbacks are not included.

Tuned for performance, AVIPs are an integral component in a simulation acceleration environment, speeding up verification 10’s to 1,000’s of times relative to simulation. The level of acceleration gain is dependent on the user’s individual testbench and DUT synchronizations.



Specification Support

This VIP supports specification versions: 1.3a and 1.4b

Usage Options

- Simulation Acceleration
- HW/SW Co-Verification

Supported Design-Under-Test Configurations

- | | | |
|--|---|-------------------------------------|
| <input checked="" type="checkbox"/> Master | <input checked="" type="checkbox"/> Slave | <input type="checkbox"/> Hub/Switch |
| <input checked="" type="checkbox"/> Full Stack | <input type="checkbox"/> Controller-only | <input type="checkbox"/> PHY-only |

Product Highlights

Supported HDMI 1.4b features:

- All extended resolution frames

All HDMI 3D frame format types, including:

- Frame packing (for both progressive and interlaced frame types)
- Side-by-side—half
- Top and bottom
- Field alternative
- Line alternative
- Side-by-side—full
- L+depth
- L+depth+graphics+graphicsdepth

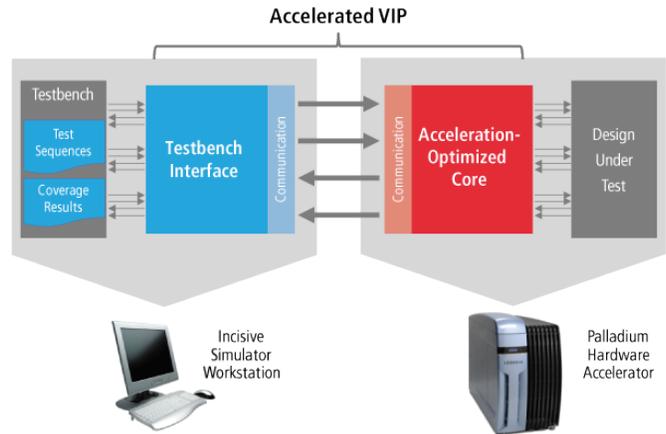
Supported HDMI 1.3a features:

- All types of data islands
- All video frame types
- All VIC values listed in CEA-861-E
- Support for full 32KB E-EDID address space
- CEC channel
- HDCP authentication/key exchange over I2C

Simulation Acceleration

In simulation acceleration, the Cadence Palladium XP system works in conjunction with the Cadence Incisive® Simulator to divide up the simulation task. The Palladium XP runs the design under test while the Incisive simulator runs the testbench. Accelerated VIP is inserted for each of the standard interfaces in the design with the testbench interface running on Incisive and the acceleration-optimized core running on the Palladium XP.

Most of the testbench components employed in simulation can be reused, which saves set-up time and preserves the controllability and observability of traditional logic simulation. With this approach, performance is often up to 1000X faster than logic simulation.



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