cādence®

Accelerated VIP for AMBA AXI

Overview

Sometimes chips are just too big to verify with logic simulation software. SoCs comprised of tens of millions of logic gates will bog down software simulators, even when running on the fastest servers.

Simulating big designs requires hardware-assisted verification, an approach that uses special-purpose hardware, like Cadence® Palladium® XP systems, to dramatically boost simulation performance.

Cadence Accelerated VIPs are complementary products to Cadence simulation VIP and SpeedBridges. Accelerated VIPs are used to funnel data to the user's design-under-test and respond to stimulus received from it. Monitor functions such as collecting coverage and setting callbacks are not included.\

Tuned for performance, AVIPs are an integral component in a simulation acceleration environment, speeding up verification 10's to 1,000's of times relative to simulation. The level of acceleration gain is dependent on the user's individual testbench and DUT synchronizations.
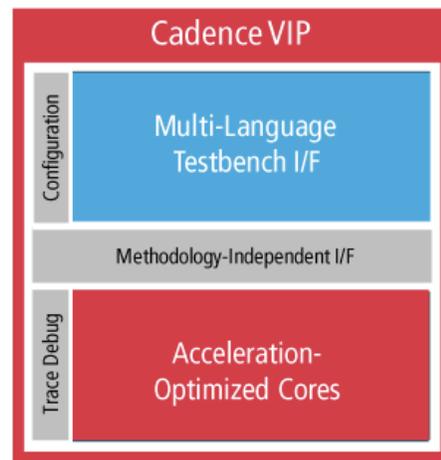
Specification Support

All AXI transactions are in accordance with the ARM AMBA AXI and ACE protocol specification for AXI3, AXI4, and AXI4-Lite, ACE and ACE-Lite.

Usage Options

- ☑ Simulation Acceleration
- ☑ HW/SW Co-Verification

Supported Design-Under-Test Configurations

☑ Master	☑ Slave	☐ Hub/Switch
☑ Full Stack	☐ Controller-only	☐ PHY-only

Product Highlights

- Generate and drive bus traffic as an AXI™ master
- Respond to bus traffic as an AXI slave
- Collect protocol coverage at the burst abstraction level when used with an e testbench.

The AXI AVIP supports all types of AXI transactions, including:

- Unaligned transfers
- Narrow transfers
- Interleaved transactions
- Outstanding transactions
- Receipt of out-of-order transactions

Simulation Acceleration

In simulation acceleration, the Cadence Palladium XP system works in conjunction with the Cadence Incisive® Simulator to divide up the simulation task. The Palladium XP runs the design under test while the Incisive simulator runs the testbench. Accelerated VIP is inserted for each of the standard interfaces in the design with the testbench interface running on Incisive and the acceleration-optimized core running on the Palladium XP.

Most of the testbench components employed in simulation can be reused, which saves set-up time and preserves the controllability and observeability of traditional logic simulation. With this approach, performance is often up to 1000X faster than logic simulation.
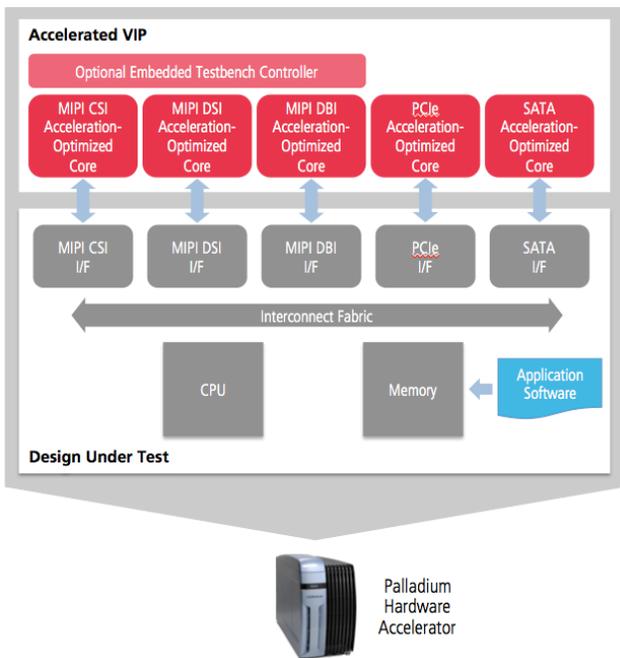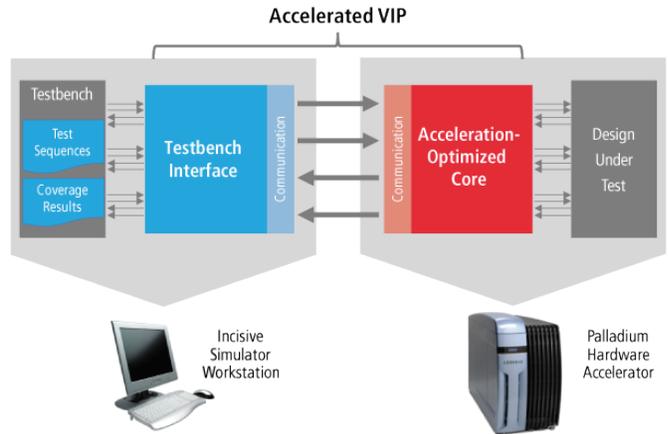
HW/SW Co-Verification

With the HW/SW co-verification approach, both the test environment and the design under test run in the Palladium XP system. This results in huge performance gains – typically 10,000X to 100,000X faster than logic simulation. That kind of speed enables the verification of software along with the hardware design. This enables hardware/software integration bugs to be efficiently discovered and fixed – a task that would be nearly impossible to manage otherwise. To facilitate the HW/SW co-verification approach, application software is often used to run tests and monitor results.

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