

# DFI Assertion-based VIP

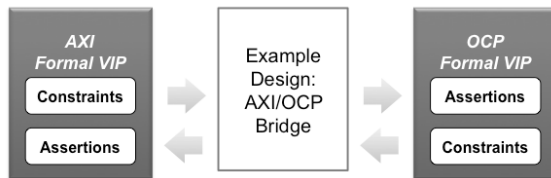
## Overview

Formal analysis is a mathematical approach to verification that has the unique ability to prove that a design is 100% correct. This method is tremendously useful, but is limited in the size and types of designs that can be verified. Still, for IP blocks with bus-style interfaces, it is an ideal verification solution.

Cadence® Assertion-Based VIP simplifies formal verification through its plug-and-play approach. Just attach the VIP to your design and run – no need for complicated tests and coverage analysis.

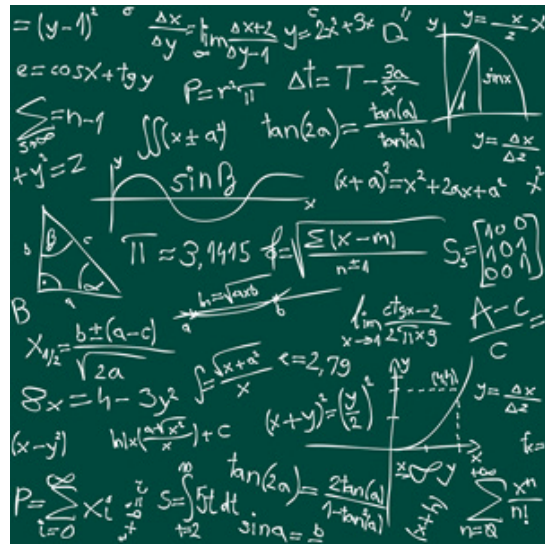
## No Tests Required

With Cadence Assertion-Based VIP, no test creation is required. Unlike logic simulation that uses test sequences to stimulate a design, a pre-programmed set of “constraints” is supplied with the assertion-based VIP. These constraints describe the range of all possible stimulus for a given interface specification. Also, “assertions” in the VIP check the interface signaling to make sure your design is acting in accordance with the protocol specification. You can start verifying your design in minutes with our assertion-based VIP.



## Debug Made Easy

Cadence Assertion-Based VIP works with the Cadence Incisive® Formal Verifier tool to make debug easy. When the VIP detects a design error, Incisive Formal Verifier displays a waveform trace, schematic view, and source code analysis of the bug. This makes it easy to find the root causes of bugs – and fix them!



## Specification Support

- The DFI ABVIP supports the DFI 2.1.1 Interface Protocol Specifications.
- The DFI3 ABVIP supports the DFI 3.0 Interface Protocol Specifications.

## Product Highlights

- Can be configured in master, slave, or monitor mode
- Master mode provides DDR memory controller capabilities to verify compliance of a DDR PHY
- Slave mode provides DDR PHY capabilities to verify compliance of a DDR memory controller
- Monitor mode provides passive checker capabilities to verify compliance of the memory controller to DDR PHY interface

## Supported Design-Under-Test Configurations

- |  |  |  |
|--|--|--|
| <input checked="" type="checkbox"/> Controller | <input checked="" type="checkbox"/> PHY  | <input type="checkbox"/> Hub/Switch          |
| <input type="checkbox"/> Full Stack            | <input type="checkbox"/> Controller-only | <input checked="" type="checkbox"/> PHY-only |