VIP Datasheet

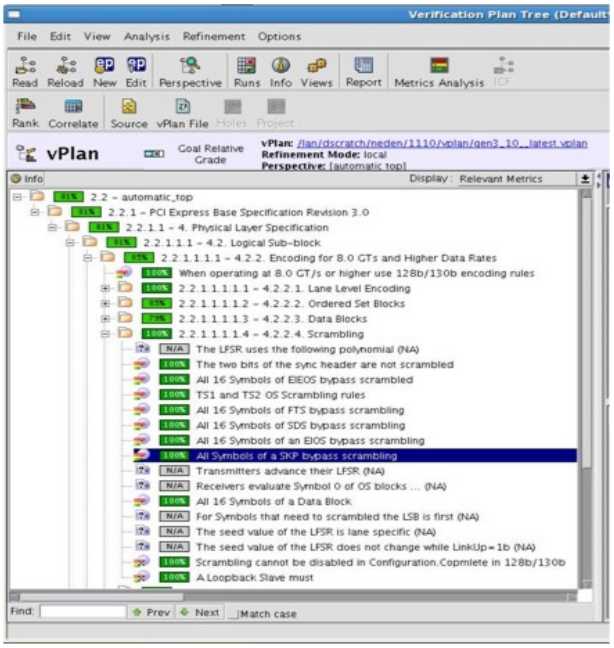
TripleCheck for PCIe

Overview

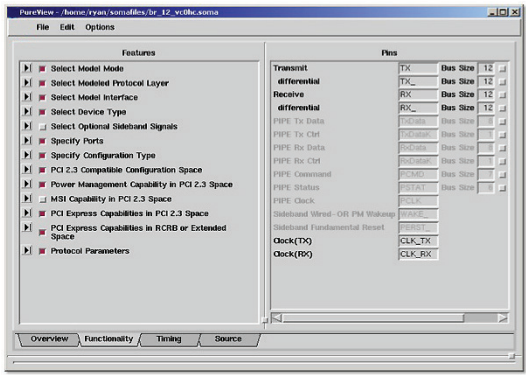
TripleCheck for PCI Express helps you verify that your design complies with the interface specification. This is different than a post-silicon compliance test that measures electrical parameters. TripleCheck works during pre-silicon logic simulation to stress-test functional behavior. TripleCheck is the third-generation compliance product to be offered by Cadence, delivering an enhanced test suite, coverage model, and verification plan.

PureView Integration

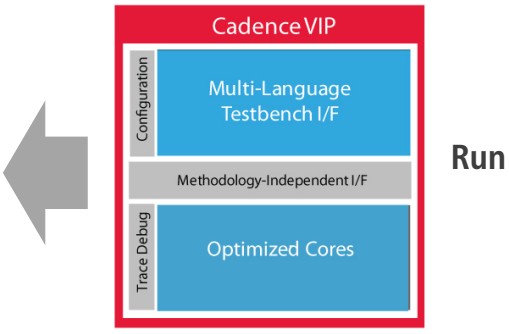
For quick set-up, TripleCheck is integrated with our PureView solution. When you configure a VIP with PureView, the TripleCheck test suite, coverage model, and vPlan are automatically configured to match the VIP.



Analyze



Configure



Run

PCIe Features

Advanced Error Reporting

Stimuli and coverage collection of all applicable error scenarios

Full LTSSM transitions

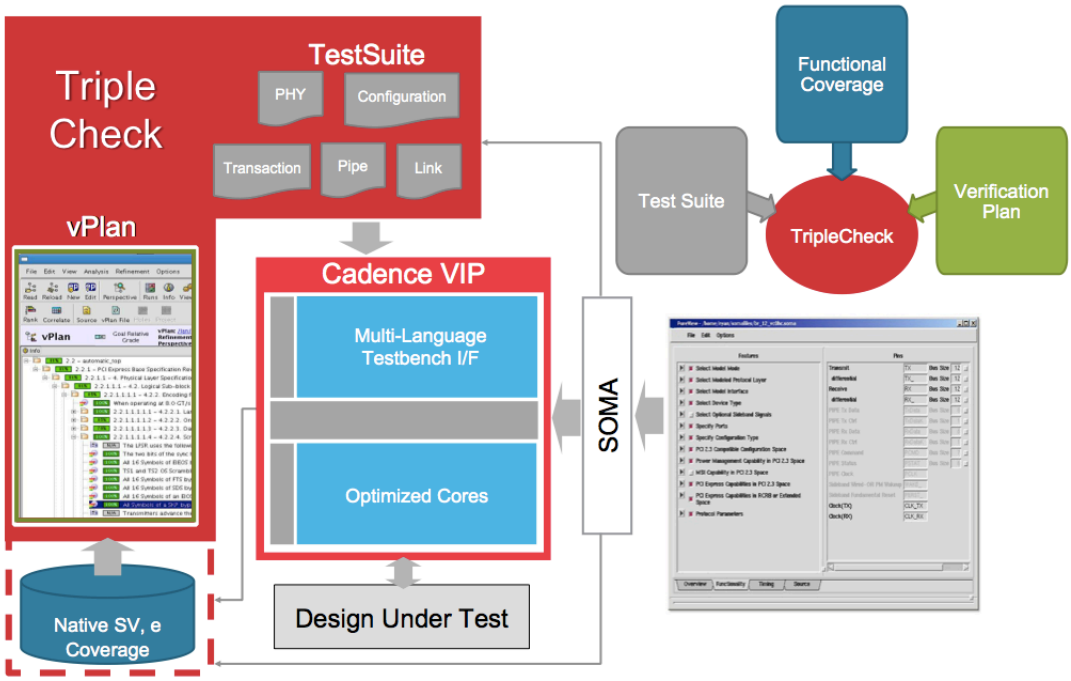
Stimuli and coverage collection of all LTSSM transitions

Equalization procedure

Stimuli and coverage collection of all aspects of Eq. process

Packet formation rules

Stimuli and coverage collection of all applicable TLPs



Test Suite

TripleCheck provides an extensive library of test sequences to stimulate the design under test. The test library contains directed tests (providing quick checks for common protocol compliance issues) as well as constrained-random test sequences for exhaustive testing to detect corner-case bugs hidden in the design. The tests support error injection in each layer of the protocol stack to check operation of the design when faced with non-compliant stimulus. This combination of directed and constrained-random tests results in high functional coverage, right out of the box.

Coverage Model

Coverage models are provided in both SystemVerilog and e verification languages. These pre-defined coverage models capture all data items and state machine transitions to track and measure verification progress. The coverage models are open and documented, which allows you to extend them with application-specific coverage definitions.

Verification Plan

TripleCheck provides a verification plan that mirrors the protocol specification. All the requirements in the protocol specification are listed in the plan and organized into the same chapter and paragraph hierarchy.

The vPlan is linked to the coverage model so that the coverage data captured during simulation runs is automatically mapped against the plan. This makes it easy to track verification progress and determine how much work remains. The vPlan is written in XML to enable portability between simulation environments.

In the Cadence® Incisive® simulation environment, TripleCheck integrates with the Incisive vManager tool to enable a number of productivity-boosting features, such as bucket analysis to analyze coverage details and test profiling to sort out unproductive test sequences.

Third-Generation Solution

TripleCheck is a third-generation pre-silicon compliance test suite solution. It combines the features from Cadence's other test suite solutions to deliver the most advanced pre-silicon compliance test suite on the market.

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