System-on-chip (SoC) verification is a big job. That’s why high-level verification languages like e and SystemVerilog were developed along with companion methodologies like the Universal Verification Methodology (UVM). But language and methodology only take you so far.

Cadence provides additional productivity-boosting tools to help you configure, run, and analyze your design. With these products, you get up and running quickly and shorten your overall verification project.

PureView is a graphical cockpit used to configure all our VIP products. Many interface protocols have dozens of configuration options. To match a VIP component to your design, each option needs to be set correctly. It would be time-consuming and error-prone to set every parameter with a text command, but PureView makes it easy. The tool walks you through a hierarchy of menus to configure a VIP component. It only shows you relevant options based on previous choices and prevents illegal settings. PureSuite is also used to configure memory model options and TripleCheck tests.