

Simulation VIP for USB 3.0

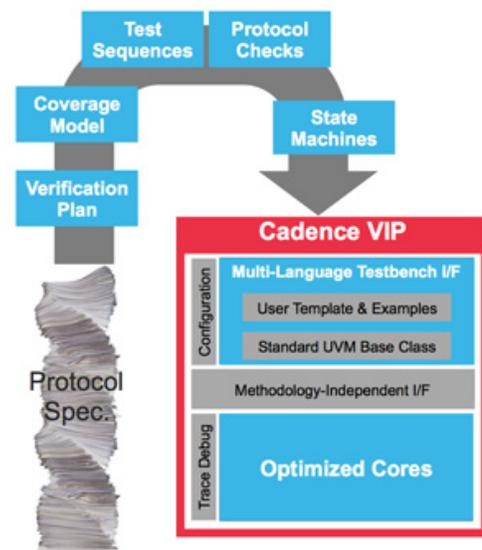
Includes support for OTG 3.0

Overview

Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

The base specifications for the USB 3.0 protocol are available here: <http://www.usb.org/developers/docs>

Product Highlights

- Includes OTG support
- Provides optional SuperSpeed Inter-Chip (SSIC) simulation VIP
- Features optional PureSuite product with extensive pre-silicon compliance tests

Supported Design-Under-Test Configurations

- | | | |
|--|---|-------------------------------------|
| <input checked="" type="checkbox"/> Master | <input checked="" type="checkbox"/> Slave | <input type="checkbox"/> Hub/Switch |
| <input checked="" type="checkbox"/> Full Stack | <input checked="" type="checkbox"/> Controller-only | <input type="checkbox"/> PHY-only |

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification.

“Cadence USB 3.0 Verification IP has enabled us to thoroughly verify that our designs comply with the USB 3.0 specification, and this new SSIC product demonstrates the company’s commitment to supporting engineers working with this key protocol. By supporting all popular verification methodologies and simulators, the Cadence VIP has enabled GUC to support our diverse customer base with high-quality SoC and IP verification coverage.”

– James Cheng, Senior Vice President, Global Unichip

Key Features

- Supports backward compatibility with USB 2.0, in high- and full-speed modes
- Supports all compliance patterns as part of compliance LTSSM state
- Supports USB 3.0 link training with all LTSSM state transitions and covers all arcs
- Supports PHY loop-back state with bit error rate test
- Supports OTG 3.0 support and role swapping protocol (RSP)
- Supports the USB 3.0 smart isochronous transfers
- Supports USB 3.0 bulk streaming protocol
- Provides a complete USB protocol hierarchy enumeration process for host and device models
- Supports link management packet flow
- Supports all low-power entry/exit sequences to U1, U2, and U3 states
- Does protocol checks at each layer, such as physical, link, protocol, and framework
- Supports spread spectrum clocking

Test Suite

This VIP includes a basic test suite capability that includes:

- 3rd party simulator test execution
- Directed compliance tests
- Constrained-random compliance tests
- Tests targeting all protocol layers
- SystemVerilog functional coverage model

Related Products

- USB 2.0 Simulation VIP



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