VIP Datasheet

Simulation VIP for USB 2.0

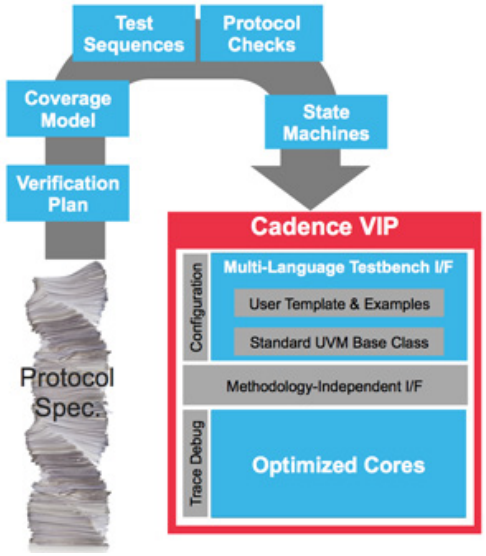
Part of a complete USB verification solution

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

The specifications for the USB 2.0 and OTG 2.0 protocols are available at http://www.usb.org/developers/docs.

Product Highlights

- Includes OTG support
- Optional SuperSpeed Inter-Chip (SSIC) simulation VIP
- Optional PureSuite product with extensive pre-silicon compliance tests

Supported Design-Under-Test Configurations

☑ Host	☑ Device	☐ Hub/Switch
☑ Full Stack	☑ Controller-only	☐ PHY-only

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the "raw" coverage model results back to the protocol specification.

"The Cadence SuperSpeed USB VIP has helped PLDA to be one of the first IP vendors to reach the market, while ensuring it is among the highest quality products available. Using Cadence VIP has enabled PLDA to achieve significantly greater functional coverage results."

– Stephane Hauradou, Chief Technology Officer, PLDA

Key Features

- Supports all types of transfers: bulk, control, interrupt, and isochronous and split transactions
- Backwards-compatible with USB 1.1 specifications
- Provides a complete USB protocol hierarchy enumeration process for host, device, and hub models
- Operates at high, full, or low speed
- Supports OTG 1.3 and OTG 2.0 revisions with both A-device and B-device configurations
- Supports SRP (session request protocol), ADP (attach detection protocol), and HNP (host negotiation protocol)
- Supports reset and high-speed chirp handshake
- Supports suspend, resume, remote wake-up, and low-power management (LPM)
- Checks for all transaction and packet rules including inter-packet gap and propagation delays
- Supports all UTMI+ levels (1, 2, 3)

Test Suite

This VIP includes a basic test suite capability that includes:

- 3rd party simulator test execution
- Directed compliance tests
- Constrained-random compliance tests
- Tests targeting all protocol layers
- SystemVerilog functional coverage model

Related Products

- USB 3.0 Simulation VIP

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