

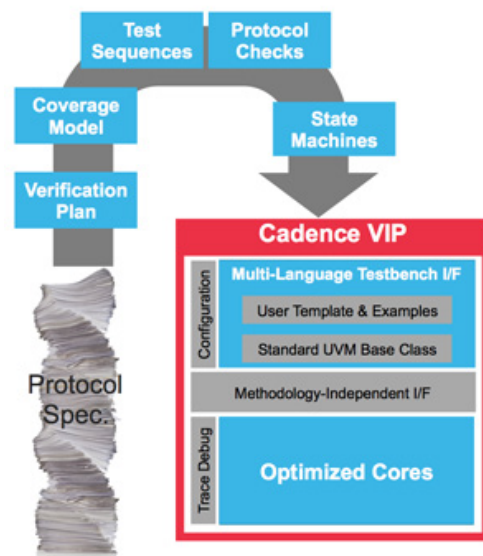
Simulation VIP for UART

Overview

Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

The UART VIP supports the standard UART 16550 Specification, available at <http://www.opencores.org>.

Supported Design-Under-Test Configurations

- | | | |
|---|--|-------------------------------------|
| <input checked="" type="checkbox"/> Transmitter | <input checked="" type="checkbox"/> Receiver | <input type="checkbox"/> Hub/Switch |
| <input checked="" type="checkbox"/> Full Stack | <input type="checkbox"/> Controller-only | <input type="checkbox"/> PHY-only |

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification.

Key Features

- Support for full-duplex asynchronous communications
- Baud rate generation subsystem
- Auto baud rate generation
- Overrun error
- RX data available
- Frame error
- TX holding register empty
- Parity error
- RX line status interrupt
- Modem status interrupt
- Configurable stop bits (1 or 2 stop bits)
- 1.5 Stop Bits for 5 bit character length
- Support for up to 128-byte transmit and receive FIFOs
- Programmable data word length (5, 6, 7, or 8 bits)
- Support for hardware flow control using RTS/CTS signals

Test Suite

This VIP includes a basic test suite capability that includes:

- Constrained-random example tests
- 3rd party simulator test execution



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