VIP Datasheet

Simulation VIP for SSIC

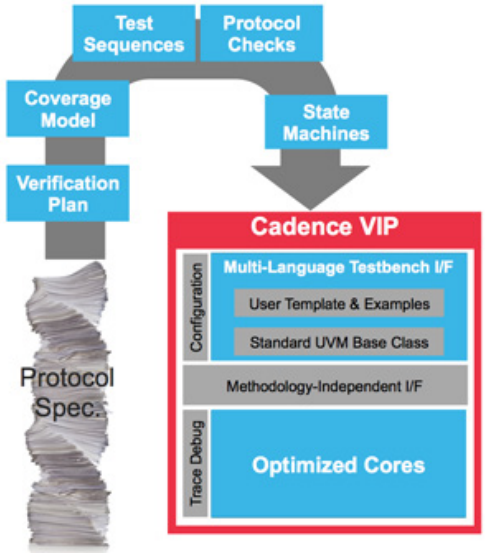
The first SuperSpeed Inter-Chip VIP

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

The base specifications for the SSIC and USB 3.0 protocols are available here: http://www.usb.org/developers/docs

Product Highlights

- Industry's first SSIC VIP

Supported Design-Under-Test Configurations

☑ Host	☑ Device	☐ Hub/Switch
☑ Full Stack	☑ Controller-only	☐ PHY-only

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the "raw" coverage model results back to the protocol specification.

Key Features

- Supports all high-speed burst gears (HS-G1/HS-G2/HS-G3) and date rate series (A/B)
- Supports low-speed burst mode called pulse-width modulation (PWM-G1)
- Supports LINE-RESET mechanism for warm reset
- Supports x1, x2, x4 lanes
- Supports remote register access protocol
- Compliant with Type-I M-PORTs from the MIPI M-PHY specifications
- Supports Loopback, Analog Loopback, and Receive Burst for x1 lane

Test Suite

This VIP includes a basic and PureSuite test suite capability that includes:

- 3rd party simulator test execution
- Directed compliance tests
- Constrained-random compliance tests
- Tests targeting all protocol layers
- SystemVerilog functional coverage model

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