Simulation VIP for SATA 6G
Trusted by dozens of customers

Overview
Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.

Specification Support
This VIP supports SATA Specification version 3.1

Product Highlights
• Features optional Accelerated VIP

Supported Design-Under-Test Configurations
- Host
- Full Stack
- Device
- Controller-only
- Port Multiplier
- PHY-only

Deliverables
People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:
• State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
• Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
• Test suites are provided for most Cadence VIP components.
• Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
• Verification plans for most protocols link the “raw” coverage model results back to the protocol specification.
**Key Features**

- Supports many feature sets and commands from ACS commands
- ATA Packet Interface Support
- Coherent read and write to different ports
- All finite state machines and state transition checks
- Supports Serial 1 bit as well parallel 10/20/40-bit interface
- Memory Subsystem: System, Buffer, and Log memory
- All the Finite state machines and state transition checks
- Multiple PRD table implementation
- Controllable protocol checkers and passive monitors
- Terminate a DMA data transmission
- Asynchronous Signal Recovery
- Device behaves as if it has multiple memory subsystems to behave as port multiplier
- Different feature configurations for each port (Eg. Port 0 ATA, Port 1 ATAPI)
- Clock recovery and speed negotiation, OOB signaling with different OOB data, signature FIS, error injection and speed up of bypass initialization
- Interface power states: Partial, Slumber, and Device Sleep
- Native Command Queueing
- Does protocol checks at each layer, such as physical, link, transport, and command
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- Send and Receive FPDMA Queued Commands

**Test Suite**

This VIP includes a basic test suite capability that includes:
- Constrained-random example tests
- 3rd party simulator test execution

**Related Protocols**

- SATA 1.5G/3G/6G Accelerated VIP