

Simulation VIP for SAS 12G

Production proven verification capability

Overview

Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

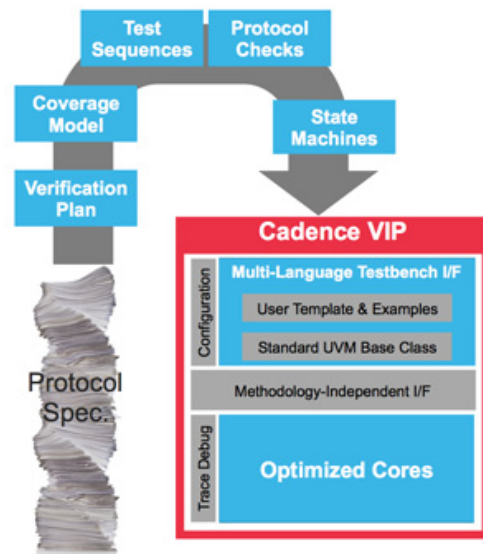
The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.

Specification Support

SAS 12G VIP supports SAS (Serial Attached SCSI) Specification revision 11-036r9.

Supported Design-Under-Test Configurations

- | | | |
|--|--|-----------------------------------|
| <input type="checkbox"/> Initiator | <input checked="" type="checkbox"/> Target | <input type="checkbox"/> Expander |
| <input checked="" type="checkbox"/> Full Stack | <input type="checkbox"/> Controller-only | <input type="checkbox"/> PHY-only |



Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification.

Key Features

- Supports arbitration between multiple OPEN address frames
- Supports BMC encoding/decoding feature of PHY
- Supports transmission and reception of error TTIUs and error response TTIUs
- Supports Frame bursting for READ/WRITE commands
- Supports verification of both INITIATOR and TARGET SAS device types
- Supports frame transmission as per interlocked and non-interlocked frame type
- Supports all LINK layer state machines for connection control, transmitter, receiver
- Supports RRDY, CREDIT_BLOCKED etc primitives which are used for flow control
- Supports PHY reset sequence, hard reset sequence, and link identification sequence
- Supports G1/G2/G3/G4 speeds (1.5/3/6/12Gbps)
- Supports all PHY/LINK layer timers
- Supports OOB sequence, Speed Negotiation Sequence
- Supports PHY training sequence at 6Gbps
- Supports PHY transmitter/receiver training sequence at 12Gbps
- Supports link rate matching feature at 1.5/3/6/12Gbps
- Supports all frame types for INITIATOR and TARGET: SSP_COMD, SSP_DATA, SSP_TASK, SSP_XFER, SSP_RESP
- Support for SPL-3 Persistent-Connection feature
- Supports SSP and SMP transport layer protocols

Test Suite

This VIP includes a basic test suite capability that includes:

- Constrained-random example tests
- 3rd party simulator test execution

Related Products

- SAS 6G Simulation VIP



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