VIP Datasheet

Simulation VIP for PCI Express Gen3

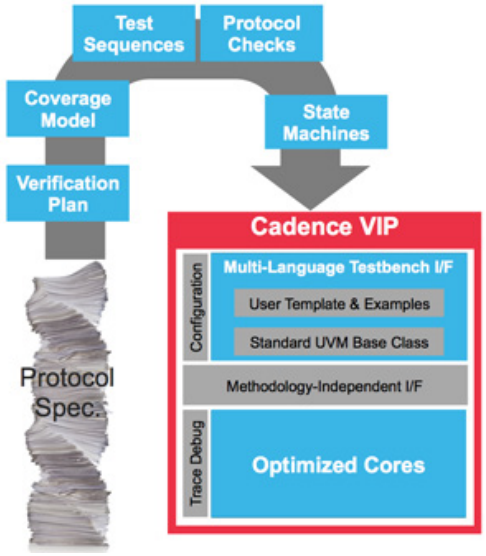
The most complete and capable PCIe 3.0 VIP

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, ***e***, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

The VIP is fully compliant with the 3.0 revision of the PCI Express spec, and the ECNs listed below.

Product Highlights

- Supports the latest specification ECNs
- OptionalTripleCheck product provides a complete pre-silicon compliance testing solution
- Features optional Accelerated VIP

Part of a complete PCIe solution including:

- PCIe Gen4
- PCIe Gen2
- NVM Express
- Mobile PCIe
- SR-IOV
- MR-IOV

Supported Design-Under-Test Configurations

☑ Root Complex ☑ End Point ☑ Switch Bridge

☑ Full Stack ☑ Controller-only ☑ PHY-only

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations
- Test suites are provided for most Cadence VIP components
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface
- Verification plans for most protocols link the "raw" coverage model results back to the protocol specification

"Wipro has been consistently enabling semiconductor companies to reduce verification time and increase coverage parameters through its next-generation frameworks and market-proven end-to-end verification services. Our partnership with Cadence has played an instrumental role in fulfilling the IP verification needs of our customers. We chose PCIe Gen3 VIP along with TripleCheck by Cadence to achieve a comprehensive solution that gives us the fastest path to IP verification closure."

– A. Vasudevan, VP Semiconductor and Systems, Wipro

Key Features

- Perform and control all equalization aspects
- Error injection, checking, and coverage
- Protocol multiplexing ECN
- ASPM optionality ECN
- Downstream port containment ECN
- PCIe over M-PHY ECN
- Precision time measurement ECN
- Full support for the new TS symbols
- New skip OS full support
- Optimized buffer flush\fill
- L1 sub states ECN
- Lightweight notification ECN
- Process address space ID ECN

Test Suite

This VIP includes a basic and TripleCheck test suite capability that includes:

- 3rd party simulator test execution
- Directed compliance tests
- Constrained-random compliance tests
- Tests targeting all protocol layers
- SystemVerilog functional coverage model
- ***e*** functional coverage model
- Verification plan mapped to protocol specification
- Verification plan integration with Cadence vManager metric-driven analysis system
- Verification plan integration with 3rd party simulator environments
- Verification plan integration with 3rd party simulator environments

Related Products

- PCIe Gen2 Simulation VIP
- PCIe Gen4 Simulation VIP
- PCIe SR-IOV Simulation VIP
- PCIe MR-IOV Simulation VIP
- NVM Express Simulation VIP
- Mobile PCI Simulation VIP
- PCIe Gen2/Gen 3 Accelerated VIP

"We've determined that 90% of the risk is in the chip's interfaces. If we design the interfaces incorrectly, it doesn't matter if we get the rest of the chip right. This is especially true with PCIe since it's such a complex protocol. The bottom line for us is that the choice we made to go with proven IP that's easy to get up and running is really just good, solid common sense."

– Jim O'Connor, Vice President of Engineering, iVivity

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