

Simulation VIP for PCI Express Gen2

The most mature PCIe VIP, used by more than 100 customers

Overview

Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.

Specification Support

This VIP is fully compliant with the 2.1 revision of the PCI Express specification.

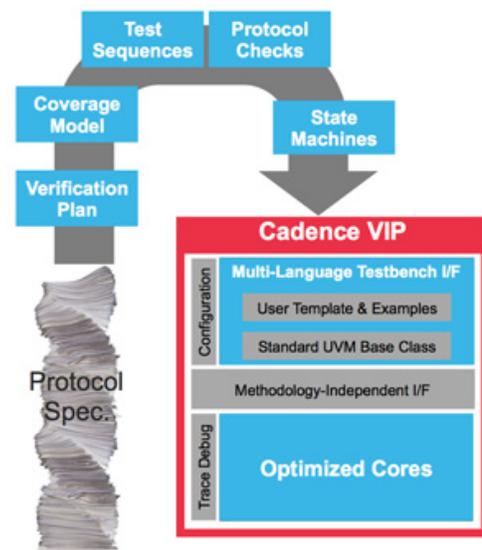
Product Highlights

Part of a complete PCIe solution including:

- PCIe Gen3
- PCIe Gen4
- NVM Express
- Mobile PCIe
- SR-IOV
- MR-IOV
- Supports the latest specification ECNs
- Optional TripleCheck product provides a complete pre-silicon compliance testing solution
- Features optional Accelerated VIP

Supported Design-Under-Test Configurations

- | | | |
|--|---|---|
| <input checked="" type="checkbox"/> Root Complex | <input checked="" type="checkbox"/> End Point | <input checked="" type="checkbox"/> Switch Bridge |
| <input checked="" type="checkbox"/> Full Stack | <input checked="" type="checkbox"/> Controller-only | <input checked="" type="checkbox"/> PHY-only |



Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations
- Test suites are provided for most Cadence VIP components
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification

“When faced with the important decision as to which IP vendor has the most reputable and silicon-proven PCIe IP, Denali (now Cadence) was the preferred vendor that met our critical high throughput and feature requirements. We rely on Cadence’s high-quality, interoperable design and verification IP solutions, and excellent customer support to meet the PCIe 2.0 and IOV specifications, our product development timeframes, and achieve a competitive advantage.”

– Jim Finnegan, Sr. Vice President of Silicon Engineering, Netronome

Key Features

- Supports x1, x2, x4, x8, x12, x16, and x32 lanes
- Complete link training status state machine (LTSSM) modeling, including all configuration, power-saving, and recovery states
- Full control of the link speed, up and down changes
- Full support for up and down configuration (link size)
- Provides a complete PCI Express protocol hierarchy enumeration process including resource allocation
- Adding skew between lanes
- Recover clock from bitstream or use reference clock
- Add jitter to the clock
- Full control of the Ack\Nak protocol and timers, predefined sequence number, link CRC (LCRC), and duplicate TL error injections
- Full control of Flow Control Credits (FCCs), including initial allocation of FCCs and the frequency of on-the-fly FCC updates
- Serial, 8-bit, 10-bit, PIPE 3.0, PIPE 4.0, PIE8
- WAKE#, CLKREQ#, PERST#
- End Point, Legacy End Point, Root Complex, Bridge, Switch, PHY-DUT
- Memory, I/O, Configuration, MSI\MSI-X
- Automatic, user-defined flow control initialization per virtual channel (VC)
- Full compliance of function level reset

Test Suite

This VIP includes a basic and TripleCheck test suite capability that includes:

- 3rd party simulator test execution
- Directed compliance tests
- Constrained-random compliance tests
- Tests targeting all protocol layers
- SystemVerilog functional coverage model
- e functional coverage model
- Verification plan mapped to protocol specification
- Verification plan integration with Cadence vManager metric-driven analysis system
- Verification plan integration with 3rd party simulator environments
- Verification plan integration with 3rd party simulator environments

Related Products

- PCIe Gen3 Simulation VIP
- PCIe Gen4 Simulation VIP
- PCIe SR-IOV Simulation VIP
- PCIe MR-IOV Simulation VIP
- NVM Express Simulation VIP
- Mobile PCI Simulation VIP
- PCIe Gen2/Gen 3 Accelerated VIP



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