VIP Datasheet

Simulation VIP for OCP 2.2

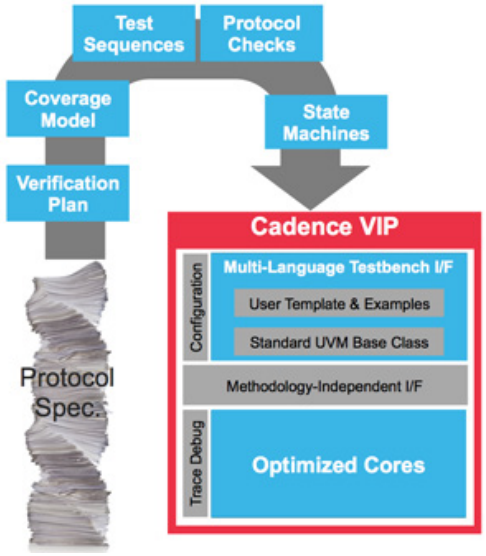
Used on over 100 design projects

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

Our OCP VIP supports the OCP protocol v2.2, which is incremental to OCP versions 2.1 and 2.2.

Product Highlights

- Features optional Assertion-Based VIP

Supported Design-Under-Test Configurations

☑ Master	☑ Slave	☐ Hub/Switch
☑ Full Stack	☐ Controller-only	☐ PHY-only

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the "raw" coverage model results back to the protocol specification.

Key Features

- Supports both the blocking and non-blocking flow control options for the requests
- Supports the enable signal for clock
- Supports connect-disconnect feature for both master and slave
- Ensures that the WriteNonPost (WRNP) and WriteConditional (WRC) commands always have responses regardless of whether write response enable has been set in the interface configuration, as defined in the OCP 2.2 specification
- Emulates the full behavior of an unlimited number of OCP masters capable of generating all types of OCP transfers, according to OCP 2.2 specification
- Supports multiple thread IDs and multiple tag IDs
- Supports out-of-order responses
- Supports request interleaving. The interleaving depth is determined from the signal, MAtomicLength
- Emulates the full behavior of an unlimited number of OCP slaves that respond to traffic over a bus, and generates all types of responses to a DUT master, according to OCP 2.2 specification
- Supports both synchronous and asynchronous reset. Also supports reset on-the-fly

Test Suite

This VIP includes a basic test suite capability that includes:

- 3rd party simulator test execution
- Tests targeting all protocol layers
- e functional coverage model
- Verification plan mapped to protocol specification
- Verification plan integration with Cadence vManager metric-driven analysis system

Related Products

- OCP 3.0

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