

Simulation VIP for Mobile PCI express

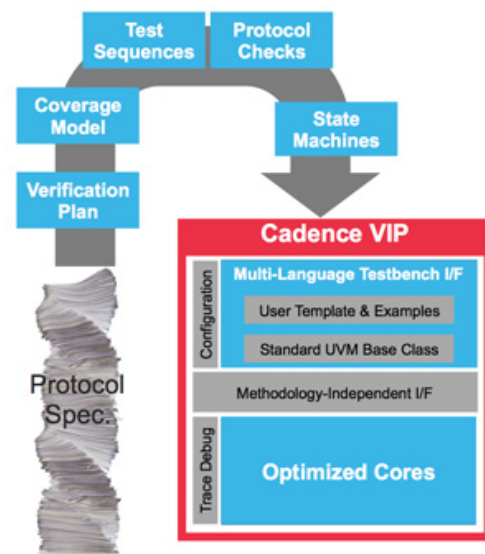
First VIP to support Mobile PCI Express

Overview

Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

The base spec for PCIe 3.0 and ECN for M-PCIe can be downloaded only by members of the PCI-SIG website: <http://www.pcisig.com/home>.

Product Highlights

Part of a complete PCI Express solution including:

- PCI Express Gen3
- PCI Express Gen2
- NVM Express
- Mobile PCI Express
- SR-IOV
- MR-IOV

Supported Design-Under-Test Configurations

- | | | |
|--|---|-------------------------------------|
| <input checked="" type="checkbox"/> Root Complex | <input checked="" type="checkbox"/> End Point | <input type="checkbox"/> Hub/Switch |
| <input checked="" type="checkbox"/> Full Stack | <input checked="" type="checkbox"/> Controller-only | <input type="checkbox"/> PHY-only |

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification.

“M-PCIe helps boost mobile device performance by delivering best-in-class, highly scalable I/O functionality, enabling the migration of business apps to smartphones and tablets as they take on the role of primary computing devices. We are delighted that Cadence is enabling SoC developers to rapidly adopt M-PCIe by delivering IP and VIP products supporting this standard.”

– Al Yanes, Chairman and President, PCI-SIG

Key Features

- Supports all High Speed burst gears(HS-G1/HS-G2/HS-G3) and data rate series(A/B)
- Supports Low Speed burst mode called Pulse Width modulation(PWM-G1)
- Supports the bandwidth reconfiguration via Recovery states
- Support x1, x2, x4, x8, x12, x16 x32 lanes
- Supports remote register access protocol
- Compliant with Type-I M-PORTs from the MIPI M-PHY specifications
- TX/RX link width can be changed via Recovery. Reconfig state
- TX and RX link width can be chosen to be different
- TX-Lanes can be directed to enter STALL in L0 state

Test Suite

This VIP includes a basic test suite capability that includes:

- Constrained-random example tests
- 3rd party simulator test execution

Related Products

- PCIe Gen4 Simulation VIP
- PCIe Gen3 Simulation VIP
- PCIe Gen2 Simulation VIP
- PCIe SR-IOV Simulation VIP
- PCIe MR-IOV Simulation VIP
- NVM Express Simulation VIP
- PCIe Gen2/Gen 3 Accelerated VIP



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