VIP Datasheet

Simulation VIP for MIPI UniPro

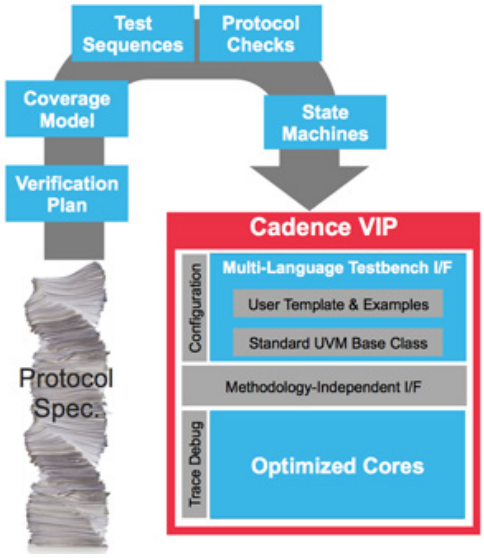
Industry's first UniPro VIP

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

The UniPro VIP supports MIPI UniPro specification, version 1.61, 1.6, and 1.41.

Product Highlights

- Industry's first UniPro VIP
- Part of the broadest line of MIPI simulation VIP
- Cadence has been a MIPI Alliance Contributing Member since 2007

Supported Design-Under-Test Configurations

☑ Master	☑ Slave	☐ Hub/Switch
☑ Full Stack	☑ Controller-only	☐ PHY-only

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the "raw" coverage model results back to the protocol specification.

Key Features

- Supports testing of 1.41 to 1.6 connection compatibility
- Supports up to four lanes: PWM G1-G7, HS G1-G3 on each direction, and A/B HS rate series
- Supports Serial and RMMI interfaces (downstream)
- Supports CPort signal interface (upstream)
- Supports PHY Adapter, Data Link, Network, and Transport layers
- PA link start up, (re-)initialization, configuration, and hibernate enter/exit sequences
- Supports DLL initialization, TC0 and TC1, flow control, and acknowledgement mechanisms
- Supports TL connection management and addressing, segmentation and reassembly, end-to-end flow control, and multi-CPort arbitration.
- Supports testing of 1.41, 1.6 and 1.61 connection compatibility.

Test Suite

This VIP includes a basic test suite capability that includes:

- Constrained-random example tests
- 3rd party simulator test execution

Related Products

- MIPI CSI-3 Simulation VIP
- MIPI C-PHY Simulation VIP
- MIPI -D-PHY Simulation VIP
- MIPI DigRF Simulation VIP
- MIPI DSI Simulation VIP
- MIPI LLI Simulation VIP
- MIPI M-PHY Simulation VIP
- MIPI SLIMbus Simulation VIP
- MIPI Soundwire Simulation VIP
- MIPI CSI-2 Accelerated VIP
- MIPI DBI Accelerated VIP
- MIPI DSI Accelerated VIP
- UFS Memory Model

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