

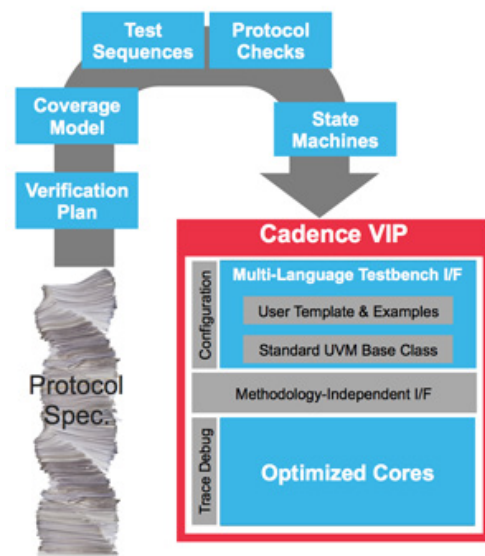
# Simulation VIP for MIPI Soundwire

## Overview

Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



## Specification Support

The SoundWire VIP supports MIPI SoundWire specification version 1.0, officially released by MIPI in February 2015.

## Product Highlights

- First to market with SoundWire VIP support
- Enables emulation with up to 11 slaves, with 1 to 14 data ports per slave
- Supports Initialization sequence and enumeration process
- Supports multi-lane configuration

## Supported Design-Under-Test Configurations

- |  |   |                                     |
|--|---|-------------------------------------|
| <input checked="" type="checkbox"/> Master     | <input checked="" type="checkbox"/> Slave | <input type="checkbox"/> Hub/Switch |
| <input checked="" type="checkbox"/> Full Stack | <input type="checkbox"/> Controller-only  | <input type="checkbox"/> PHY-only   |

## Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification.

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## Key Features

- Support in a limited set of values of the WordLength field
- High-Performance PHY.
- Master assigns Dev\_num for each newly attached slave.
- Frame size and DP channels can be switched during activity.
- Master and Slave can generate error scenarios.
- Dynamic addition and removal of Slave devices.
- Support of static and PRBS data payload sending.
- Monitor can take command ownership from Master.
- Slave and Master devices support Bulk Payload Transport Protocol.
- Support in Full, Reduced and Simplified Data Ports
- Up to 8 data lanes are supported.
- Sync slave with master SoundWire frame.
- Slave and Master devices can send data payload traffic.
- Ability to perform all kinds of resets on the fly.
- Slave VIP replies automatically when interrupt needs to be generated based on configuration.
- Master can access slave registers through broadcast and multicast.
- Slave VIP automatically replies with appropriate command responses.
- Slave and Master devices can send asynchronous data payload traffic.
- Master device supports PHY Test Modes

## Test Suite

This VIP includes a basic test suite capability that includes:

- Constrained-random example tests
- 3rd party simulator test execution

## Related Products

- MIPI CSI-3 Simulation VIP
- MIPI C-PHY Simulation VIP
- MIPI -D-PHY Simulation VIP
- MIPI DigRF Simulation VIP
- MIPI DSI Simulation VIP
- MIPI LLI Simulation VIP
- MIPI M-PHY Simulation VIP
- MIPI SLIMbus Simulation VIP
- MIPI UniPro Simulation VIP
- MIPI CSI-2 Accelerated VIP
- MIPI DBI Accelerated VIP
- MIPI DSI Accelerated VIP
- UFS Memory Model



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