

# Simulation VIP for MIPI SLIMbus

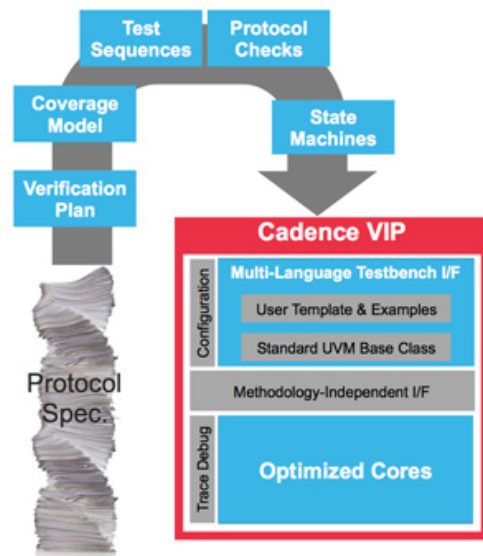
Used on dozens of MIPI verification projects

## Overview

Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



## Specification Support

The VIP supports the latest version of the SLIMbus specification.

## Product Highlights

- Industry’s first SLIMbus VIP
- Part of the broadest line of MIPI simulation VIP
- Cadence has been a MIPI Alliance Contributing Member since 2007

## Supported Design-Under-Test Configurations

- |                                                    |                                                   |                                     |
|----------------------------------------------------|---------------------------------------------------|-------------------------------------|
| <input checked="" type="checkbox"/> Active Manager | <input checked="" type="checkbox"/> Generic Devic | <input type="checkbox"/> Hub/Switch |
| <input checked="" type="checkbox"/> Full Stack     | <input type="checkbox"/> Controller-only          | <input type="checkbox"/> PHY-only   |

## Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification.

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## Key Features

- Supports up to 8 data lines.
- Supports SLIMbus transport protocols (Isochronous, Pushed, Pulled, Async Simplex, Async half-duplex, Extended Async).
- Provides ability to change root freq and clock gear.
- Supports all kinds of protocol resets.
- Supports the active framer handover flow.
- Supports data carrying on multiple channels that have the same direction and sample rate and that are phase-aligned.
- Supports all protocol messages.
- Supports component boot-up sequence and recovery of sync loss.
- Supports information/value element messages.
- Supports all roles of Active Framer (Framing Channel and clocks).
- Supports Clock Pause flows.

## Test Suite

This VIP includes a basic and CMS test suite capability that includes:

- Constrained-random compliance tests
- Tests targeting all protocol layers
- 3rd party simulator test execution
- e functional coverage model
- Verification plan mapped to protocol specification
- Verification plan integration with Cadence vManager metric-driven analysis systems

## Related Products

- MIPI CSI-2 Simulation VIP
- MIPI CSI-3 Simulation VIP
- MIPI C-PHY Simulation VIP
- MIPI -D-PHY Simulation VIP
- MIPI DigRF Simulation VIP
- MIPI DSI Simulation VIP
- MIPI LLI Simulation VIP
- MIPI M-PHY Simulation VIP
- MIPI Soundwire Simulation VIP
- MIPI UniPro Simulation VIP
- MIPI CSI-2 Accelerated VIP
- MIPI DBI Accelerated VIP
- MIPI DSI Accelerated VIP
- UFS Memory Model



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