

Simulation VIP for MIPI M-PHY

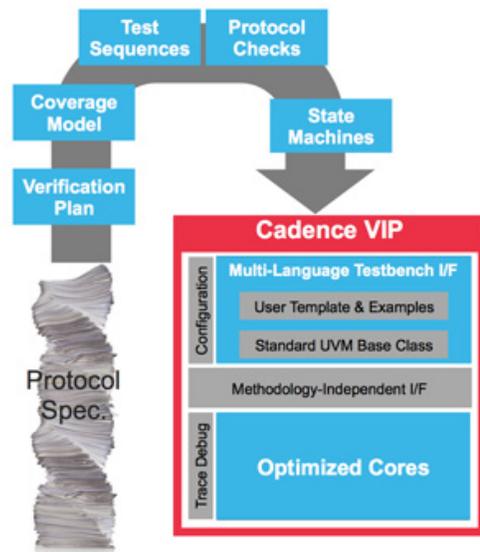
First production of MIPI M-PHY

Overview

Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

This VIP supports specification version: 3.1 and below

Product Highlights

- Industry’s first M-PHY VIP
- Part of the broadest line of MIPI simulation VIP
- Cadence has been a MIPI Alliance Contributing Member since 2007

Supported Design-Under-Test Configurations

- | | | |
|--|---|--|
| <input checked="" type="checkbox"/> Master | <input checked="" type="checkbox"/> Slave | <input type="checkbox"/> Hub/Switch |
| <input type="checkbox"/> Full Stack | <input type="checkbox"/> Controller-only | <input checked="" type="checkbox"/> PHY-only |

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification.

“Mobile device users demand ever-increasing power-efficiency, and the MIPI Alliance chip-to-chip interfaces are an essential low-power technology for smartphone and tablet developers. As an early contributing member of the MIPI Alliance, Cadence has helped speed the adoption of mobile specifications, now including the M-PHY-based M-PCIe.”

– Joel Huloux, Chairman of the Board, MIPI Alliance

Key Features

- Supports distribution and merging data over one to four lanes. Also supports a different number of lanes per sub-link (direction)
 - Supports Type 1 and Type 2
 - Supports Burst state, ACTIVATED SAVE states (SLEEP and STALL) and hibernate (“HIBERN8”) state
 - Supports multiple transmission speed ranges (PWM G1-G7, all Hs-GEARs) and rates per BURST mode
 - Complies with MIPI M-PHY 3.0 specification
 - Supports serial interface (DpDn) and signaling interface (RMMI)
 - Supports multiple transmission modes with different bit-signaling and clocking schemes
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Test Suite

This VIP includes a basic test suite capability that includes:

- Constrained-random example tests
- 3rd party simulator test execution

Related Products

- MIPI CSI-2 Simulation VIP
- MIPI CSI-3 Simulation VIP
- MIPI C-PHY Simulation VIP
- MIPI -D-PHY Simulation VIP
- MIPI DigRF Simulation VIP
- MIPI DSI Simulation VIP
- MIPI LLI Simulation VIP
- MIPI SLIMbus Simulation VIP
- MIPI Soundwire Simulation VIP
- MIPI UniPro Simulation VIP
- MIPI CSI-2 Accelerated VIP
- MIPI DBI Accelerated VIP
- MIPI DSI Accelerated VIP
- UFS Memory Model



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