

Simulation VIP for MIPI LLI

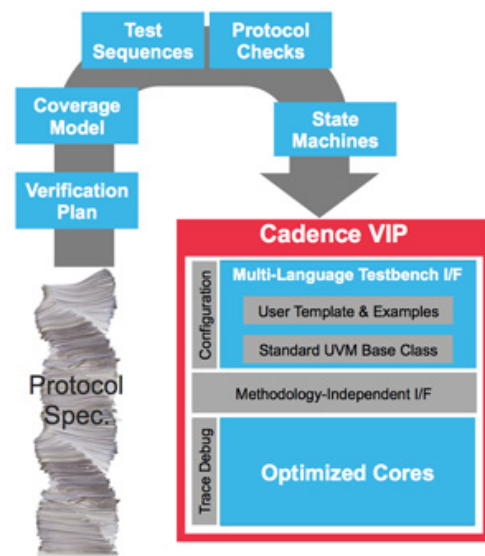
The world's first LLI VIP

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

The LLI VIP supports MIPI Low-Latency Interface specification version 2.0.

Product Highlights

- First to market with LLI 2.0 VIP support
- Supports extended data frames (PHIT36)
- Supports automatic scrambling
- Provides Interconnect Adaptation Layer (IAL) with AMBA® AXI

Supported Design-Under-Test Configurations

- | | | |
|--|---|-------------------------------------|
| <input checked="" type="checkbox"/> Master | <input checked="" type="checkbox"/> Slave | <input type="checkbox"/> Hub/Switch |
| <input checked="" type="checkbox"/> Full Stack | <input checked="" type="checkbox"/> Controller-only | <input type="checkbox"/> PHY-only |

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification.

Key Features

- Complies with MIPI LLI specification version 2.0
- Supports PHY, PA, DLL, and transport layers
- Supports PA PHIT, CRC, and SEQ automatic calculation and generation
- Supports PHIT36 (extended data frames)
- Supports DLL message and transaction frame
- Supports DLL flow control and mount/unmount procedure
- Supports protocol TCs
- Supports all types of TL_IC and TL_SVC packets
- Supports retransmission queue
- Includes the MIPI M-PHY VIP for PHY verification
- Supports Interconnect Adaptation Layer (IAL) with AMBA® AXI
- Supports scrambling

Test Suite

This VIP includes a basic test suite capability that includes:

- Constrained-random example tests
- 3rd party simulator test execution

Related Products

- MIPI CSI-2 Simulation VIP
- MIPI CSI-2 Accelerated VIP
- MIPI CSI-3 Simulation VIP
- MIPI DBI Accelerated VIP
- MIPI C-PHY Simulation VIP
- MIPI DSI Accelerated VIP
- MIPI -D-PHY Simulation VIP
- UFS Memory Model
- MIPI DSI Simulation VIP
- MIPI DigRF Simulation VIP
- MIPI M-PHY Simulation VIP
- MIPI SLIMbus Simulation VIP
- Simulation VIP MIPI Soundwire
- MIPI UniPro Simulation VIP



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