VIP Datasheet

Simulation VIP for MIPI CSI-2 v2.0

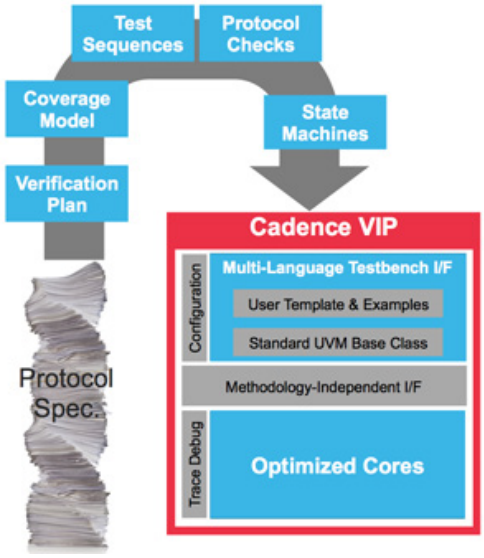
Includes D-PHY and C-PHY

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

The CSI-2 v2.0 VIP supports the following draft specifications:

MIPI CSI-2 Specification v. 2.0 r02

MIPI D-PHY Specification, v. 2-0 r06

MIPI C-PHY Specification, v. 1-1 r04

Product Highlights

- Industry's first CSI-2 VIP
- Part of the broadest line of MIPI simulation VIP
- Features optional Accelerated VIP
- Cadence has been a MIPI Alliance Contributing Member since 2007

Supported Design-Under-Test Configurations

☑ Master	☑ Slave	☐ Hub/Switch
☑ Full Stack	☑ Controller-only	☐ PHY-only

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the "raw" coverage model results back to the protocol specification.

Key Features

- Supports continuous TxWordClkHS and RxWordClkHS clock operation
- Supports RAW16 and RAW20 data types
- Supports both D-PHY 1.2 and C-PHY 1.0 with both PHY interfaces (DpDn and PPI)
- Verifies both CSI-2 receiver and transmitter
- Includes the MIPI D-PHY and C-PHY VIPs for physical layer verification
- Supports virtual channel and data type interleaving
- Supports all 4 trigger commands, including low-power data after trigger transmission and low-power data pause
- Supports injection of errors in the CSI-2, D-PHY and C-PHY layers
- Supports pixel-to-byte packing
- Supports merging multiple packets from the same frame in a single HS burst with protocol generated and consumed fillers and spacers over C-PHY and D-PHY
- Supports 16- and 32-bit PPI data bus width over C-PHY; Supports 8-, 16- and 32-bit PPI data bus width over D-PHY
- Supports up to 32 virtual channels over C-PHY and 16 virtual channels over D-PHY
- Includes the MIPI D-PHY and C-PHY VIPs for physical layer verification.
- Supports D-PHY2-0 r06 and C-PHY1-1 r04 with both PHY interfaces (DpDn and PPI)
- Supports one to eight D-PHY data lanes
- Supports Ultra-Low Power mode (ULPM) on clock and data lanes
- Supports D-PHY and C-PHY (DpDn and PPI) event notifications for scoreboarding
- Supports pixel layer for RGB, RAW and YUV422 data types
- Supports lane based data payload scrambling as per CSI2-v2.0 specification

Test Suite

This VIP includes a basic and CMS test suite capability that includes:

- Constrained-random compliance tests
- Tests targeting all protocol layers
- 3rd party simulator test execution
- ***e*** functional coverage model
- Verification plan mapped to protocol specification
- Verification plan integration with Cadence vManager metric-driven analysis systems

Related Products

- MIPI CSI Simulation VIP (includes D-PHY)
- MIPI CSI-2 Accelerated VIP
- MIPI CSI-3 Simulation VIP
- MIPI C-PHY Simulation VIP

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