VIP Datasheet

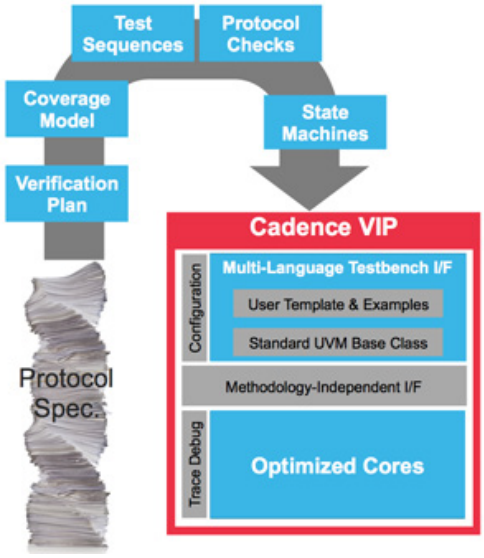
Simulation VIP for MIPI C-PHY

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

The C-PHY VIP supports MIPI C-PHY specification Version 1.0 - 05 August 2014.

Product Highlights

- First to market with C-PHY VIP support
- Supports Low and High Speed transactions
- Supports multi-lane configuration
- Built-in integration with the CSI-2 VIP

Supported Design-Under-Test Configurations

☑ Transmitter	☑ Receiver	☐ Hub/Switch
☑ Full Stack	☑ Controller-only	☐ PHY-only

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the "raw" coverage model results back to the protocol specification.

Key Features

- Supports transmitting and receiving C-PHY High Speed transactions
- Supports all parts of HS transaction (Preamble -> Sync Pattern -> data -> Post pattern
- Supports driving and detecting Sync Symbol during HS transaction
- Supports transitions from LP to HS and vice versa
- Supports 1 to 4 lanes
- Supports an API to inject CPHY symbol errors (wrong symbol/ missing symbol)
- Supports injection and detection of optional user programmable sequence as part of the HS preamble
- Supports CPHY Protocol Phy Interface - data bus of 16 bits, additional txsendsynchs and rxinvalidcodehs pins
- Supports CPHY level checkers on the sensor (master DUT)

Test Suite

This VIP includes a basic test suite capability that includes:

- Constrained-random example tests
- 3rd party simulator test execution

Related Products

- MIPI CSI-2 Simulation VIP
- MIPI CSI-3 Simulation VIP
- MIPI -D-PHY Simulation VIP
- MIPI DSI Simulation VIP
- MIPI DigRF Simulation VIP
- MIPI LLI Simulation VIP
- MIPI M-PHY Simulation VIP
- MIPI SLIMbus Simulation VIP
- MIPI Soundwire Simulation VIP
- MIPI UniPro Simulation VIP
- MIPI CSI-2 Accelerated VIP
- MIPI DBI Accelerated VIP
- MIPI DSI Accelerated VIP
- UFS Memory Model

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