VIP Datasheet

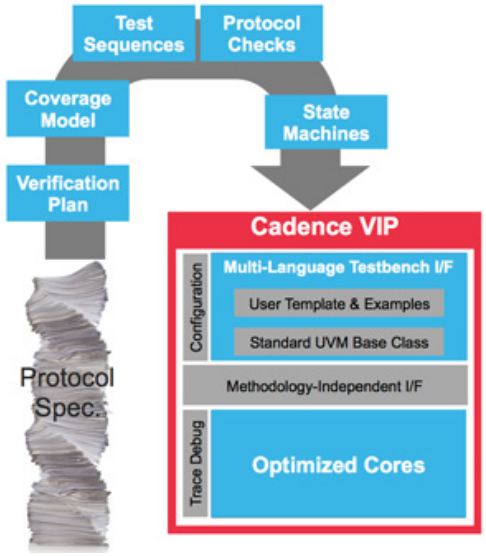
Simulation VIP for I2C

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

The I2C VIP supports the I2C Protocol v1.0, v2.0, v2.1, v3.0, and v5.0 as defined in the I2C Protocol Specification.

Product Highlights

- Features optional Accelerated VIP

Supported Design-Under-Test Configurations

☑ Master	☑ Slave	☐ Hub/Switch
☑ Full Stack	☐ Controller-only	☐ PHY-only

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the "raw" coverage model results back to the protocol specification.

Key Features

- Supports both multi-mastering and any number of slaves
- Master arbitration is supported
- Stretching of the SCL clock
- Configurable option to use for slave addressing
- Optional command support, configurable for each slave
- Sending of optional start byte in transactions is available
- All speed modes are supported: Standard, Fast, Fast Plus and High Speed
- Supports optional glitch handling
- Implements user control of slave response fields such as data, slave busy, slave sending NACK, etc.
- Optional software reset command is supported
- Optional command device ID is supported

Test Suite

This VIP includes a basic test suite capability that includes:

- 3rd party simulator test execution
- Constrained-random compliance tests
- Tests targeting all protocol layers
- e functional coverage model
- Verification plan mapped to protocol specification
- Verification plan integration with Cadence vManager metric-driven analysis system

Related Protocols

- I2C Accelerated VIP
- I2S Accelerated VIP

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