VIP Datasheet

Simulation VIP for Ethernet 40G/100G

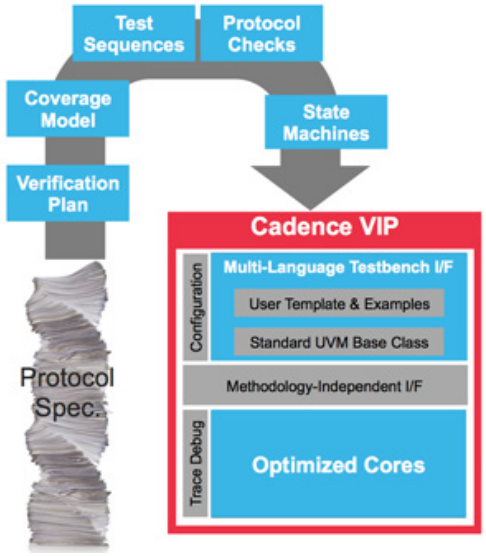
Supports Energy Efficient Ethernet (EEE)

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

This VIP supports Autonegotiation, PMD Link Training, FEC, EEE, 25G MAC support, 40GBASE-R, CGMII, and 100GBASE-R interfaces.

The Ethernet specifications are developed and maintained by IEEE.

Product Highlights

- Supports broadest range of MAC interfaces
- Supports Energy-Efficient Ethernet, Priority-Based Flow Control, and Ethernet Audio/ Video

Supported Design-Under-Test Configurations

☑ MAC	☑ PHY	☐ Hub/Switch
☑ Full Stack	☐ Controller-only	☐ PHY-only

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the "raw" coverage model results back to the protocol specification.

Key Features

- User-configurable CRC field
- Option to send an Ethernet Packet without Preamble, supported for limited interfaces
- Link level flow control for each Class of Service (CoS) as defined by IEEE P802.1p
- Flow control mechanism in which overwhelmed network element sends a Pause frame which halts the transmission for a specified period of time.
- FEC appends to the Ethernet frame additional data that is a result of set of non-binary arithmetic functions performed on the data of the Ethernet frame. This additional data (known as the FEC parity octets) is used to correct errors at the receiving end of the link that may occur when the data is transferred through the link.
- EEE is a set of enhancements to the twisted-pair and backplane Ethernet family of computer networking standards that allow for less power consumption during periods of low data activity, per Standard IEEE 802.3az.
- Serial bus defined for Ethernet family PHY's registers read and write.
- Allows custom field insertion anywhere inside the frame, staring from SFD till CRC field
- Allows customization of VLAN tags
- Allows configuration of number of bytes in a CRC field
- Auto-negotiation of 1000BASEX PHYs
- Auto-negotiation for Ethernet backplane interfaces
- Allows insertion of a message inside the Ethernet frame
- Custom preamble replaces the standard preamble of 7 bytes, and Start Frame Delimiter with a random pattern header of n number of bytes, where n is configurable
- Active, passive configuration
- 802.3, MAGIC, JUMBO, PAUSE, PFC-PAUSE, VII, SNAP
- Tagged Frame - Single Tagged(Q-VLAN tag), Double tagged(S-VLAN tag and Q-VLAN tag)
- Speed of Operation: 10 Mbps, 100 Mbps, 1 Gbps, 10 Gbps, 20Gbps, 25Gbps, 40Gbps, 100Gbps
- PMD link training as described in Clause 72 of IEEE 802.3
- Transport, network, Mpls, Snap and PTP
- Ethernet frames can be encrypted/decrypted with a user-defined 256/128-bit secure association key based on default cipher suites GCM-AES-256/128. Frames can be integrity or confidentiality protected.

Test Suite

This VIP includes a basic test suite capability that includes:

- 3rd party simulator test execution
- Directed compliance tests
- Constrained-random compliance tests
- Tests targeting all protocol layers
- SystemVerilog functional coverage model
- ***e*** functional coverage model

Related Products

- Ethernet 10/100/10G/100G Simulation VIP
- Ethernet 25G/50G Simulation VIP
- Ethernet 10/100/1G/10G Accelerated VIP

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