VIP Datasheet

Simulation VIP for DisplayPort

Supports DisplayPort and embedded DisplayPort

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

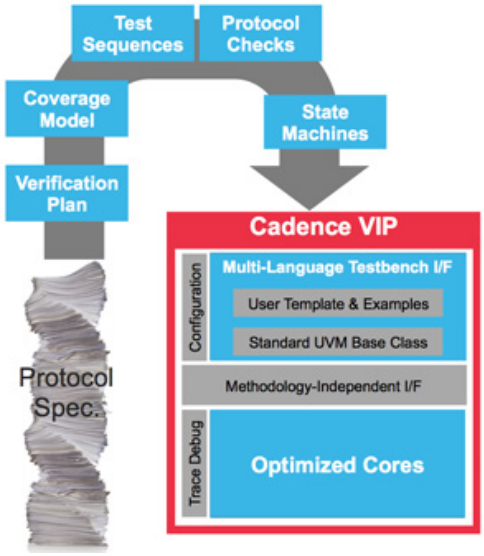
The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.

Specification Support

This VIP supports specification versions: DP 1.2, eDP 1.3, eDP 1.4, and myDP.

Supported Design-Under-Test Configurations

☑ Master	☑ Slave	☐ Hub/Switch
☑ Full Stack	☐ Controller-only	☐ PHY-only



Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the "raw" coverage model results back to the protocol specification.

Key Features

- Supports Native AUX and I2C-over-AUX
- Provides support for AUX jitter generation and detection
- Provides support for DisplayPort Configuration Data (DPCD) v1.2
- Supports both basic framing as well as enhanced framing with increased robustness
- Supports link quality measurement patterns: Nyquist, Symbol Error Rate, PRBS7, Custom 80 Bit, and HBR2 EYE pattern
- Full link training and status monitor, including clock recovery and channel equalization sequences
- Enables link re-training on loss of clock lock, symbol lock, or inter-lane alignment
- Provides main link scrambling and de-scrambling, ANSI 8B10B encoding/decoding, serialization, and deserialization
- Supports x1, x2, and x4 lane configurations
- Enables backlight and display control registers
- Supports fast training without AUX handshakes
- Supports Advanced Link Power Management (ALPM) to reduce wake latency
- Supports increased voltage swing range, allowing lower swing levels
- Enables AUX Manchester-II encoding, start and stop conditions
- Handles all pixel bit widths
- Supports secondary data error correcting code (ECC)
- Supports HPD plug, unplug, hot plug, and IRQ
- Models High Bit Rate 2 (HBR2) 5.4Gbps, High Bit Rate (HBR) 2.7Gbps, and Reduced Bit Rate (RBR) 1.62Gbps modes
- Adjustable link rates, drive voltage swing levels, and pre-emphasis levels
- Supports isochronous transport services in Single Stream Transport (SST) mode
- Enables insertion and verification of Main Stream Attributes (MSA) and Secondary Data Packet (SDP)
- Enables sink power state machine and power-save mode
- Supports Alternative Scrambler Seed Reset (ASSR)
- Provides the ability for Panel Self Refresh (PSR)
- Supports new standard link rates: R216 (2.16Gbps), R243 (2.43Gbps), R324 (3.24Gbps), and R432 (4.32Gbps) for system optimization

Test Suite

This VIP includes a basic test suite capability that includes:

- Constrained-random example tests
- 3rd party simulator test execution

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