Overview

Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.

Specification Support

The AXI VIP supports the AMBA® AXI Protocol v1.0 and v2.0 and the AXI as defined in the AMBA AXI Protocol Specification.

Product Highlights

- Part of a complete AMBA verification solution including Interconnect Verification
- Features optional Assertion-Based VIP and Accelerated VIP

Supported Design-Under-Test Configurations

- AXI3 Master
- AXI3 Slave
- AXI3 Int. Slave
- AXI3 Int. Master
- AXI4 Master
- AXI4 Slave

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification.
“HiSilicon is a leader in ASICs and solutions for communication networks and digital media. Delivering advanced multi-core ARM SoCs to our customers requires leading IC design technologies. The Cadence VIP for AXI4 and ACE enables us to quickly and efficiently deliver bug-free SoC designs.”

– Ting Lei, Director of Cloud Computing, HiSilicon

Key Features

- The user can set the VIP as active or passive without changing the testbench.
- Supports all legal data and address widths.
- Supports AxQOS, AxREGION, and user-defined signals.
- Allows AXI4 Lite configuration; automatically modify the agent accordingly.
- Configurable option to use automatic slave responses.
- User can control the order of transmission of write transfers (AXI3 only), read transfers and write responses.
- Supports sending of data before address transactions when legal.
- Sets the delay between the items on the channels
- Supports monitoring and driving of all exclusive transactions
- Supports monitoring and driving of locked transactions (AXI3 only)
- Supports both LPI controller and LIP peripheral agents
- Determines the values of the signals in the read and write address channel
- Determines the values of the signals in the write data channel
- Can support any number of agents
- Determines the values of the signals in the read data channel
- Supports monitoring and driving of all read and write transactions.

Test Suite

This VIP includes a basic and CMS test suite capability that includes:
- Constrained-random compliance tests
- Tests targeting all protocol layers
- 3rd party simulator test execution
- e functional coverage model
- Verification plan mapped to protocol specification
- Verification plan integration with Cadence vManager metric-driven analysis systems

Related Products

- AMBA 5 CHI Simulation VIP
- AMBA 4 Stream Simulation VIP
- AMBA AHB Simulation VIP
- AMBA 4 ACE Assertion-Based VIP
- AMBA AHB Assertion-Based VIP
- AMBA AXI Assertion-Based VIP
- AMBA 4 ACE Accelerated VIP
- AMBA AXI Accelerated VIP
- AMBA AHB Accelerated VIP
- AMBA APB Accelerated VIP
- Interconnect Validator (Basic)
- Interconnect Validator (Coherent)
- Interconnect Workbench