VIP Datasheet

Simulation VIP for AMBA® AHB

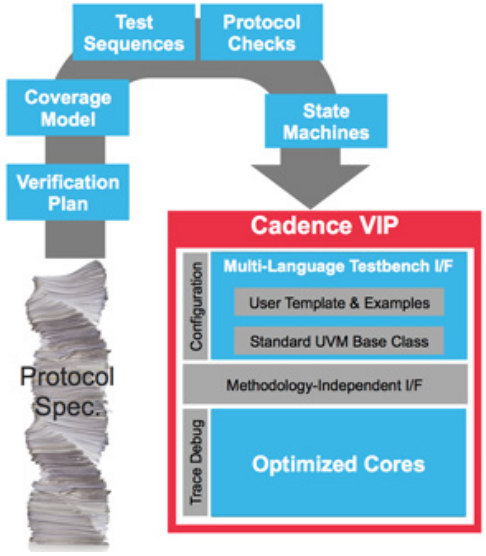
Proven on hundreds of chip designs

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

The AHB VIP supports the following official specifications:

- AMBA Specification v2.0
- AMBA 3 AHB-Lite Protocol specification v1.0
- AMBA 5 AHB5 specification update
- ARMv6 AMBA Extensions

The APB VIP supports the following official specifications:

- AMBA 2 APB Protocol specification
- AMBA 3 APB specification update
- AMBA 4 APB specification update

Supported Design-Under-Test Configurations

- ☑ Master
- ☑ Slave
- ☑ Decoder
- ☑ Arbiter
- ☑ Lite-Master

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the "raw" coverage model results back to the protocol specification.

Key Features

- The user can set the VIP as active or passive without changing the test bench, and determine, during run time, which instance to instantiate.
- Supports all legal data and address widths.
- Configurable option to use automatic slave responses.
- Set the delay between the items on the channels.
- Determine the values of the signals in the read and write address channel.
- Determine the values of the signals in the write data channel.
- Memory can be set using backdoor access.
- Can support any number of agents.
- Easy testing of error scenarios.
- Determine the values of the signals in the read data channel.
- Data consistency check for slaves using memories.
- Supports monitoring and driving of all read and write transactions.
- Configurable tracking of all the transactions on the channels.
- To handle unaligned accesses and mixed-endian accesses, enables the use of byte lane strobes to indicate which byte lanes are active in a transfer.
- Support OKAY, ERROR, SPLIT and RETRY.
- Support retraction as defined in cortex M3 spec.

Test Suite

This VIP includes a basic and CMS test suite capability that includes:

- Constrained-random compliance tests
- Tests targeting all protocol layers
- 3rd party simulator test execution
- ***e*** functional coverage model
- Verification plan integration with Cadence vManager metric-driven analysis systems

Related Products

- AMBA 5 CHI Simulation VIP
- AMBA 4 Stream Simulation VIP
- AMBA AXI Simulation VIP
- AMBA 4 ACE Assertion-Based VIP
- AMBA AHB Assertion-Based VIP
- AMBA AXI Assertion-Based VIP
- AMBA 4 ACE Accelerated VIP
- AMBA AXI Accelerated VIP
- AMBA AHB Accelerated VIP
- AMBA APB Accelerated VIP
- Interconnect Validator (Basic)
- Interconnect Validator (Coherent)
- Interconnect Workbench

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