VIP Datasheet

Simulation VIP for AMBA 5 CHI

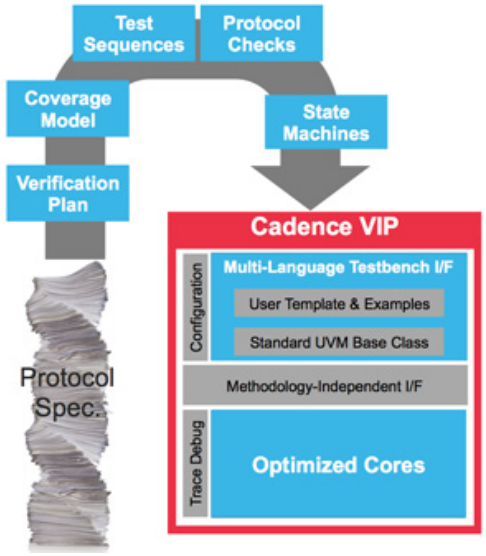
Builds on the industry's most trusted AMBA VIP solution

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

The CHI VIP supports the CHI™ Architecture Specification, issue A and the CHI™ Enhancement Specification, Version 6.0.

Product Highlights

- Supports link, network and protocol layer communication, including flow control mechanisms, across all RnX-to-HnX and HnX-to-SnX links
- Models the cache in RnF-to-HnF link
- Each link can take the part of either node as an active agent generating requests/snoops and responding according to the requests sent its way, or as a passive agent monitoring protocol correctness and collecting functional coverage

Supported Design-Under-Test Configurations

- ☑ Home Node
- ☑ Request Node
- ☑ Slave Node
- ☑ Miscellaneous Node

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the "raw" coverage model results back to the protocol specification.

Key Features

- The user can set the VIP as active or passive without changing the testbench, and determine, during run time, which instance to instantiate.
- Supports monitoring and driving of all protocol Opcodes, including barrier, exclusive access, and DVM.
- Supports monitoring and driving of all CHI.B Opcodes, including Atomic operations, Cache Stashing and Fwd snoops.
- When interconnect is not present, the Active Hn-F can generate snoop requests and respond to Rn-F commands.
- Supports link, network and protocol layer communication.
- Support for Rn-F/Rn-D/Rn-I to Hn-F/Hn-D/Hn-I/Mn and Hn-F/Hn-I/Mn to Sn-F/Sn-I.
- The user can configure the interface for node ID width, address width, data width, RSVDC width, DataCheck support and Poison support.
- Flow control mechanisms available across all RnX-to-HnX and HnX-to-SnX links.
- Specific or random values can be sent to the cache at the beginning of a test or during run time.
- User can delay the driving of all protocol flits.
- Facilitates the role of actual cache used in a CHI Rn-F.
- Facilitates the role of actual slave main memory.
- Specific or random values can be sent to the cache or main memory at the beginning of a test or during run time.

Test Suite

This VIP includes a basic test suite capability that includes:

- Constrained-random example tests
- 3rd party simulator test execution

Related Products

- AMBA 4 Stream Simulation VIP
- AMBA AHB Simulation VIP
- AMBA AXI Simulation VIP
- AMBA 4 ACE Assertion-Based VIP
- AMBA AHB Assertion-Based VIP
- AMBA AXI Assertion-Based VIP
- AMBA 4 ACE Accelerated VIP
- AMBA AXI Accelerated VIP
- AMBA AHB Accelerated VIP
- AMBA APB Accelerated VIP
- Interconnect Validator (Basic)
- Interconnect Validator (Coherent)
- Interconnect Workbench

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