

Simulation VIP for AMBA® 4 Stream

Overview

Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

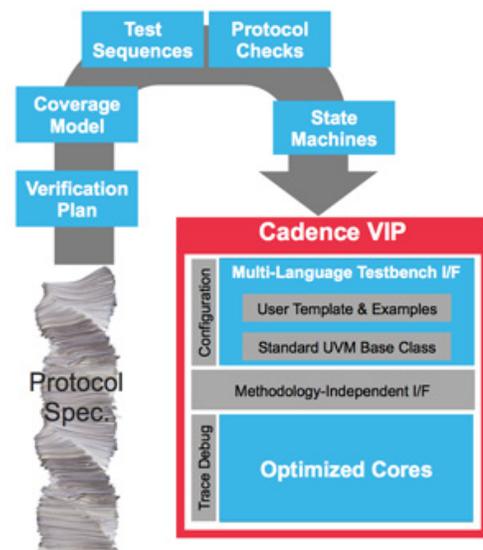
The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.

Specification Support

The AXI4-Stream VIP supports the AMBA® AXI4-Stream Protocol v1.0 and the AXI4-Stream as defined in the AMBA AXI4-Stream Protocol Specification.

Supported Design-Under-Test Configurations

- Master
- Slave



Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification.

“As the complexity of ARM partners’ designs increases year after year, successfully verifying the performance of the SoCs has become a critical imperative. The comprehensive Cadence verification IP solution for AMBA protocols has enabled our mutual customers to address this challenge while incorporating the latest ARM technology. ARM’s partnership with Cadence helps customers achieve continued success as they roll out next-generation designs incorporating our most advanced AMBA specifications such as AXI4 and AXI Coherency Extensions (ACE).”

– Joe Convey, Director of Design Enablement, ARM

Key Features

- Customizable address and data width up to 32 bits
- Sets the delay between the items on the interface
- Determines the values of the signals in the write data channel
- Order in the interface is fully controllable by the user
- Determines the values of the signals in the interface
- Can support any number of agents

Test Suite

This VIP includes a basic test suite capability that includes:

- Constrained-random example tests
- 3rd party simulator test execution

Related Products

- AMBA 5 CHI Simulation VIP
- AMBA AHB Simulation VIP
- AMBA AXI Simulation VIP
- AMBA 4 ACE Assertion-Based VIP
- AMBA AHB Assertion-Based VIP
- AMBA AXI Assertion-Based VIP
- AMBA 4 ACE Accelerated VIP
- AMBA AXI Accelerated VIP
- AMBA AHB Accelerated VIP
- AMBA APB Accelerated VIP
- Interconnect Validator (Basic)
- Interconnect Validator (Coherent)
- Interconnect Workbench



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