VIP Datasheet

Simulation VIP for AMBA 4 ACE

The first and most widely used ACE VIP

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.

Specification Support

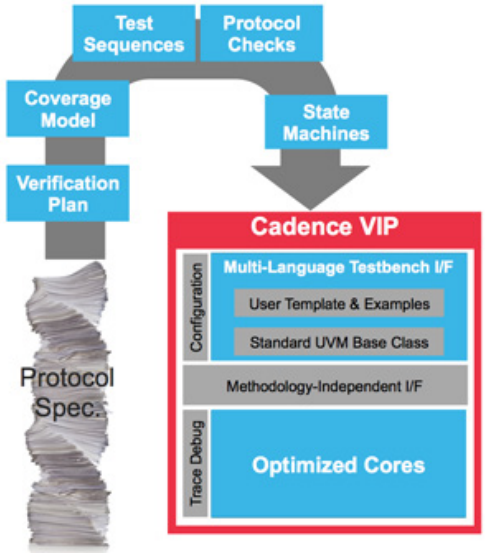
The ACE VIP supports the AMBA® ACE Protocol V1.0 and V2.0. It extends the AXI VIP which supports the AMBA® AXI Protocol v1.0 and v2.0 and the AXI as defined in the AMBA AXI Protocol Specification.

Product Highlights

- The first and most widely used ACE VIP
- Includes support for AXI 4, AXI 3, and APB
- Part of a complete AMBA verification solution including Interconnect Verification
- Features optional Assertion-Based VIP and Accelerated VIP

Supported Design-Under-Test Configurations

- ☑ Master
- ☑ Slave
- ☑ ACE-lite Master
- ☑ ACE-lite Slave



Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the "raw" coverage model results back to the protocol specification.

"Delivering advanced multi-core ARM SoCs to our customers requires leading IC design technologies. Cadence VIP for AXI4 and ACE enables us to quickly and efficiently deliver bug-free SoC designs."

– Ting Lei, Director of Cloud Computing, HiSilicon

Key Features

- The user can set the VIP as active or passive without changing the testbench.
- Supports all legal data and address widths.
- Configurable option to use automatic slave responses.
- Cache model in both active and passive agents including cache state checks.
- Supports sending of data before address transactions when legal.
- Supports monitoring and driving of DVM transactions.
- Supports both LPI controller and LPI peripheral agents.
- Determine the values of the signals in the write data channel.
- Determines the values of the signals in the snoop address channel.
- Allows ACE Lite configuration; automatically modify the agent accordingly.
- Supports the entire AXI spec. All AXI transactions can be sent and monitored.
- Supports monitoring and driving of Barrier transactions.
- User can control the order of transmission of read transfers and write responses.
- Set the delay between the items on the channels.
- Supports monitoring and driving of all exclusive transactions.
- Determine the values of the signals in the read and write address channel.
- Determine the values of the signals in the snoop response channel.
- Can support any number of agents.

Test Suite

This VIP includes a basic test suite capability that includes:

- Constrained-random example tests
- 3rd party simulator test execution

Related Products

- AMBA 5 CHI Simulation VIP
- AMBA 4 Stream Simulation VIP
- AMBA AHB Simulation VIP
- AMBA AXI Simulation VIP
- AMBA 4 ACE Assertion-Based VIP
- AMBA AHB Assertion-Based VIP
- AMBA AXI Assertion-Based VIP
- AMBA 4 ACE Accelerated VIP
- AMBA AXI Accelerated VIP
- AMBA AHB Accelerated VIP
- AMBA APB Accelerated VIP
- Interconnect Validator (Basic)
- Interconnect Validator (Coherent)
- Interconnect Workbench

"As the complexity of ARM partners' designs increases year after year, successfully verifying the performance of the SoCs has become a critical imperative. The comprehensive Cadence verification IP solution for AMBA protocols has enabled our mutual customers to address this challenge while incorporating the latest ARM technology."

– Joe Convey, Director of Design Enablement, ARM

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