TECH BRIEF

THE IMPORTANCE OF A VERIFICATION STRATEGY AND VERIFICATION IP IN SOC DESIGN

The growth of design reuse is resulting rise in the percentage of silicon occupied by IP blocks. While this trend dramatically simplifies design tasks, it results in a dramatic increase in the effort required for functional verification. Verifying today's multi-million gate SoCs requires a new verification strategy and verification IP created with reuse in mind. This technology brief focuses on a reuse approach that spans from block- to chip- to system-level verification, and ensures reusability of verification IP, environments, and plans.

During the 1990s, the electronics industry realized that available silicon area was growing faster than engineers could fill it by using custom-crafted designs. The proliferation of design reuse helped to shrink this gap and-once standards emerged for sharing and reusing design-set the stage for the commercial IP industry to flourish.

Today, the vast majority of die area is filled with reused IP blocks. While this trend has considerably reduced design effort per transistor, it has had inverse effect on the effort required for functional verification. In fact, since all the IP blocks must be integrated and verified within the context of each unique SoC, verification has become the dominant task in today's SoC and systems projects.

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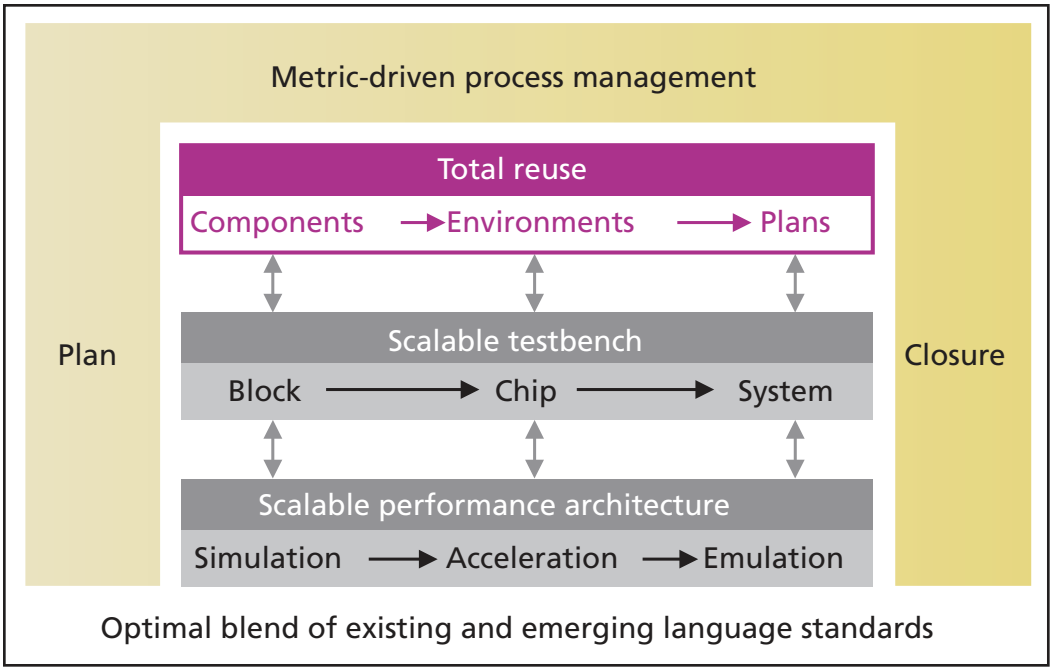

Figure 1: Reuse methods: reuse that spans verification IP, environments, and plans

To cope with the challenges of verifying multi-block, multi-million gate SoCs, design teams require a verification reuse strategy, including a sound methodology as well as verification IP specifically designed for reuse. Design IP providers try to address this need by creating associated Bus Functional Models (BFMs) and a selection of directed tests. While these offer a solution for verifying the functioning of the IP block itself, simple BFMs are not effective for SoC and/or system verification. By design, they do not interact with other verification IP and cannot perform the corner-case testing required to ensure correct operation of the full SoC. Additionally, you cannot reuse simple BFMs in derivative projects.

Verification IP reusability is critical to increasing verification efficiency and productivity. Verification IP must be created with reuse in mind to ensure that it can achieve the following goals:

1. Be easily reconfigured to move from block- to chip- to system-level verification and/or to derivative designs
2. Must plug and play and enable synchronized DUT stimulation in coordination with other verification IP
3. Must provide an executable verification plan to guide the team employing it
4. Must provide coverage metrics to achieve functional verification closure

AN ADVANCED APPROACH TO VERIFICATION REUSE

Cadence offers an extensive e-based methodology to enable and promote reuse of verification IP-including stimulus, coverage and verification plans. The core of this approach is embodied in the *e* Reuse Methodology (*e*RM), which is used by verification teams to maximize reusability of their proprietary verification environments. *e*RM also plays a critical role when verification IP is acquired from suppliers outside the verification team. *e*RM compliant e Verification Components (*e*VCs) will plug and play in any *e*RM environment by design. This capability drastically reduces the effort required to reuse externally supplied *e*VCs. In fact, *e*VCs have become the de facto standard for verification IP delivery. Every year, hundreds of *e*VCs are delivered by Cadence customers, partners, IP suppliers, and Cadence itself. This methodology and other unique aspects of this reuse approach are detailed below:

Advantages of an *e* reuse methodology
1. Extensibility of the *e* language facilitates adapting verification IP to new applications
2. *e*RM defines a resuse methodology and rules across both environments and verification IP to ensure consistency and reusability
3. Broad availability of commercially available *e*VCs from Cadence and Cadence partners
4. Allows reuse of executable verification plans (vPlans) for verifying derivative designs

Figure 2: Advantages of an e reuse methodology

ADVANTAGES OF THE CADENCE *e* REUSE METHODOLOGY

1. EXTENSIBILITY OF THE *e* LANGUAGE FACILITATES ADAPTING VERIFICATION IP TO NEW APPLICATIONS

The features of the ***e*** language's Aspect Oriented Programming (AOP) facilitate reuse by making it easy to customize and control existing verification IP. Specifically, rather than requiring edits to the original verification IP, a unique extend construct allows designers to keep the changes required to accommodate a derivative design in an external "extension file." In this way, each update to the original verification IP can be automatically incorporated in the derivative IP, thus eliminating the need to repeatedly edit in the changed code. This capability goes far beyond the simple "inheritance" feature of other object-oriented verification languages that still require extensive editing in order to reuse code.

In addition, the powerful sequence construct provides a standard means to capture and reuse stimuli from unit to chip to system level, and enables synchronized stimulus generation from multiple Verification IPs. Sequences are used to generate a wide range of complex scenarios in order to realistically exercise the Design Under Test (DUT). Multi-channel sequences can even inject stimuli across multiple interfaces simultaneously.

2. eRM ESTABLISHES REUSE METHODOLOGY AND RULES ACROSS BOTH VERIFICATION ENVIRONMENTS AND COMPONENTS, AND SPECIFIES:

- Standard format, naming and control mechanisms that simplify configuration and integration. When using either legacy verification components or those provided by third parties, learning to use each one can represent a time consuming process. eRM specifies a common look and feel for all components, including standardized naming conventions, directory structures, organization of data structures, and documentation structures. This approach makes it much easier to understand and integrate existing verification IP. In addition, eRM also makes it easy to control error messages and debug services by specifying how to encapsulate them in a single, consistent way — e.g., turning trace messages on or off with a global switch.
- Common, modular software architecture that enables reuse from unit- to system-level verification. eRM specifies how constraints, sequences, coverage, and checkers are organized so that those at the unit or block level can be easily reused when connected into the next level of integration. eRM-compliant components can be easily synchronized and controlled to create complex sequences across multiple interfaces, and, thereby, stress corner cases. The sequence construct in e is instrumental in enabling this aspect of reuse.
- Consistent coverage/metric guidelines to support coverage closure. The coverage description is an inherent part of eRM. It provides the verifier of an IP block a view of the quality of the block when used either stand-alone or in-system context. Hooks for additional coverage goals can be added to adapt the IP to a particular application. The coverage metric for each verification component can then be automatically rolled up into an overall view of coverage to help guide the team's verification efforts towards less verified portions of the system. By following the eRM, teams can have confidence that the specification of coverage will be consistent across the project.

Note: eAnalyzer is a Cadence product that performs an eRM compliance check on a verification environment to enforce the eRM guidelines.

3. INDUSTRY ACCEPTANCE HAS LED TO BROAD AVAILABILITY OF LEGACY AND COMMERCIAL VERIFICATION IP

Based on the widespread adoption of Specman Elite and eRM, users around the world have developed over 800 reusable eVCs. These eVCs promote reuse within individual companies as well as with their business partners. There are also dozens of commercially supplied eVCs offered by Cadence and its partners. These eVCs are available for critical protocols such as PCI Express, AMBA AHB and AMBA AXI, PCI, Ethernet, USB, SATA, and OCP.

4. EXECUTABLE VERIFICATION PLANS (VPLANS) CAN BE REUSED TO VERIFY ENTIRE CHIPS/SYSTEMS AND DERIVATIVE DESIGNS

A vPlan is provided with Cadence verification IP to guide the verification effort for each protocol or block. Used together with vManager it enables the team to create a reusable and executable specification of their coverage goals. Since it is executable, it guides the verification process by further automating functional verification closure. A vPlan can also be created for any individual verification IP or for the entire verification environment. For example, vPlans for unit-level tests can be included in higher level vPlans for full chip/system verification. Similarly much of the vPlan created for a brand new design can be reused for verifying derivative designs.

REUSE IS KEY TO VERIFICATION PRODUCTIVITY AND QUALITY

Adopting a verification reuse methodology and leveraging existing verification components wherever possible are the two best ways to improve verification productivity and quality. They accelerate the time to first simulation and provide the most efficient path from unit-level verification to full-chip or system-level, leveraging the preceding work at each stage.

The Cadence reuse methodologies, together with its supporting technology and ready-made verification IP with built-in vPlans, provide the most comprehensive approach to reuse available in the industry. Moreover, it is the only methodology that supports reuse of verification IP, environments and verification plans, and spans all the way from the block to chip and system-level verification. eRM compliant verification components meet all the requirements for reuse, and can be easily reconfigured for derivative designs, coexist and synchronize with other verification IP, and provide coverage metrics required for functional verification closure. Verification IP reuse is indeed the best weapon to combat skyrocketing complexity. The Cadence VPA solution is built to take full advantage of reuse at every stage of the verification process and has a 2–3 year lead over all competing solutions.

For more information about this and other products contact:

info@cadence.com

or log on to:

www.cadence.com

cadence™

Cadence Design Systems, Inc.

CORPORATE HEADQUARTERS
2655 Seely Avenue
San Jose, CA 95134
P: +1.800.746.6223 *(within US)*
+1.408.943.1234 *(outside US)*
F: +1.408.943.5001
www.cadence.com

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