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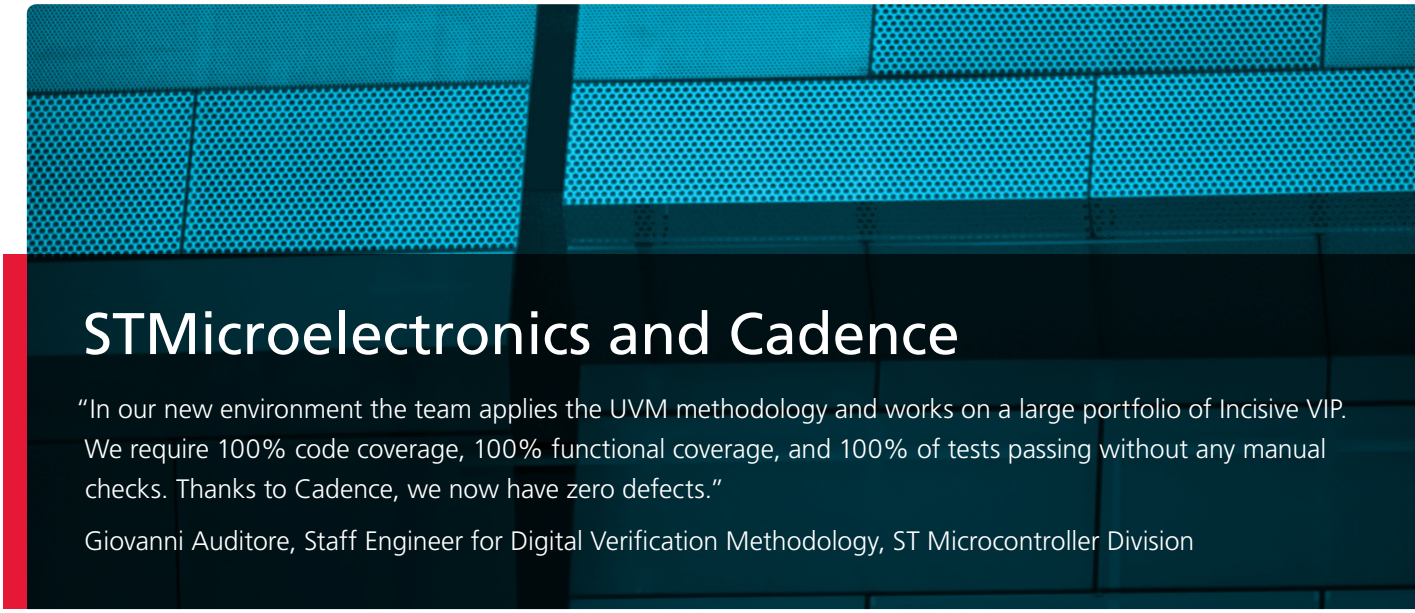

STMicroelectronics and Cadence

"In our new environment the team applies the UVM methodology and works on a large portfolio of Incisive VIP. We require 100% code coverage, 100% functional coverage, and 100% of tests passing without any manual checks. Thanks to Cadence, we now have zero defects."

Giovanni Auditore, Staff Engineer for Digital Verification Methodology, ST Microcontroller Division

The Customer

STMicroelectronics (ST) is a world-leading integrated device manufacturer providing semiconductor solutions for all electronics segments. ST is a technology innovator with more than 20,000 patents, and its key strengths are in the areas of multimedia convergence, power applications, and sensors. The company offers a rich, balanced portfolio of systems on chips (SoCs), application-specific integrated circuits (ASICs), application-specific standard products, and multi-segment products.

The ST Microcontroller Division is responsible for the company's STM32 family of 32-bit flash microcontrollers based on the ARM Cortex-M processor. This product family offers high performance, real-time capabilities, digital-signal processing, and low-power, low-voltage operation—combined with full integration and ease of development. The wide range of available STM32 devices, based on an industry-standard core and accompanied by tools and software, makes them ideal for small projects or entire platforms.

The Challenge

Because the STM32 processors cover a large range of industry uses, they come with many interfaces and protocols and contain both analog and digital intellectual property (IP). For this reason the team's digital IP verification needs have changed dramatically over the past several years.

Until early 2006, the team relied on VHDL directed testbench verification that was implemented and run by the IP developer, and the average verification effort took 35 weeks. Verification reuse was difficult due to lack of standards and the absence of a reuse methodology. At this time ST management decided to

Business Challenge

- Increasing time-to-market pressure for high-quality microcontrollers

Design Challenges

- Needed an enhanced, accelerated methodology to verify digital IP components
- Required a more effective verification reuse methodology
- Required 100% code coverage, 100% functional coverage, and 100% of tests passing without any manual checks

Cadence Solutions

- Incisive Enterprise Simulator
- Incisive Enterprise Specman Elite Testbench
- Incisive SimVision
- Incisive Enterprise Verifier
- Incisive Enterprise Manager
- Incisive Verification IP (VIP)
- Accellera Systems Initiative Universal Verification Methodology (UVM)

Results

- Reduced the average verification effort for a new digital IP from 35 weeks to 25 weeks, speeding time to market
- Achieved zero-defect delivery
- Met stringent quality goals early in verification process

build a dedicated IP verification team. Giovanni Auditore, Staff Engineer for Digital Verification Methodology, ST Microcontroller Division, was hired to help build a new, more efficient verification approach.

"Our focus shifted toward developing existing IPs with enhanced specs and imported IPs with quality-assessment requirements," Auditore says. "The pressure to work quickly and get to market fast with a high-quality product increased and verification reuse became our first priority. We no longer had time for code errors."

The team needed an enhanced methodology to verify digital IP components at a very high level. Then it would only have to check the correctness of the integration in the SoC, as opposed to performing IP verification at this late stage.

The Solution

Using Cadence® Incisive® Verification IP (VIP), the ST Microcontroller Division has successfully transformed its methodology to meet today's digital verification requirements. The team's average verification effort now takes 25 weeks for new digital IPs, compared to the previous 35 weeks. The number of bugs discovered after sign-off is 0.06, or two bugs in 30 projects. This translates into a 30% productivity gain in verification compared to previous projects as a result of adopting Incisive functional verification portfolio solutions.

> *"We spend about 40% to 50% of our entire verification effort in debug. That means that during this six-month verification project, we spent about three months in debug. Using Specman and SimVision played a large role in helping us achieve a zero-defects product."*

"In our new environment the team applies the UVM methodology and works on a large portfolio of Incisive VIP," Auditore says. "We require 100% justified code coverage, 100% functional coverage, and 100% of tests passing with no visual checks. Thanks to Cadence, we now have zero defects."

Back in 2007, the division's verification flow was loosely integrated with multiple electronic design automation (EDA) vendor products, which affected overall productivity by slowing down the verification process. Today, the verification flow relies completely upon the Incisive functional verification solution, including Incisive Enterprise Simulator, Enterprise Specman® Elite® Testbench, SimVision, Incisive Enterprise Verifier, and Incisive Enterprise Manager. The Incisive flow has eliminated the integration complexity and provided massive productivity gains.

When the design group first started verification with the full Cadence solution, its target was flow optimization to achieve fast verification closure and ease of reuse. It quickly met this goal.

"We achieved this target by adhering to the Cadence verification flow and driving it in cooperation with Cadence CustomerSupport, which provided feedback and suggestions based on real project experience," Auditore says. "This cooperation has contributed significantly to our team's productivity."

Having succeeded in this first targeted area, the team's second target was a zero-defects delivery. The team achieved this as well, by efficiently using several different Cadence verification solutions that worked synergistically within a strong metric-driven verification (MDV) methodology. One key solution was SimVision, which helped remove the debug bottleneck from ST's verification process.

"We spend about 40% to 50% of our entire verification effort in debug," Auditore says. "That means that during this six-month verification project, we spent about three months in debug. Specman and SimVision played a large role in helping us achieve a zero-defects product."

With Enterprise Specman Elite Testbench, the team now uses executable specifications and designer-specified constraints to automate testbench generation while simultaneously finding problems in the specifications. This solution's automated data and assertion checking speeds debug, while its functional coverage analysis capability drives verification using the MDV methodology.

"Incisive Specman technology supports industry-standard verification languages and is compatible with the Accellera Systems Initiative UVM, so our engineers can quickly integrate it with established verification flows," Auditore says. "We have greatly improved our functional coverage by extending it to ***e*** language, which we feel offers the highest levels of security and speed."

In some cases the team also performs formal verification with Incisive Enterprise Verifier using Property Specific Language (PSL) assertions. This solution has helped the ST Microcontroller Division locate otherwise easy-to-miss bugs when using stand-alone formal or simulation—leading to quality improvements. Incisive Enterprise Verifier enabled the integration of formal analysis methods with dynamic simulations.

Cadence solutions helped the ST team improve code-coverage results using the Incisive Metric Center as well as the AMBA High-performance Bus (AHB) VIP and vr_ad packages. The ST team also used Incisive Enterprise Manager to view and analyze the test stimulus results, which functioned in parallel to running full regressions. This approach allowed a more intuitive feature by feature view of verification artifacts at multiple levels of abstraction, namely block, chip, system and project level analysis.

"We use Specman with VHDL and PSL assertions for formal verification," Auditore adds. "This is important because different approaches take different levels of effort and it might be convenient in some cases to compress the required time for a project delivery."

Thanks to Cadence verification solutions, the design team can now use a unified coverage-driven approach that includes both dynamic and static methods. This is important because although Specman and formal methods are complementary, it can be difficult to certify what has been verified by which approach. This makes it hard to define the correct bandwidth to reduce verification overlapping and make sure there are no gaps.

Summary

With Cadence Incisive VIP, the ST methodology is centered on the verification plan. It's based on a consolidated verification environment structure that enables fast integration of both internal and external verification components and ease of verification reuse. It's also highly configurable and takes advantage of the fast verification feedback provided by the static property checking approach and the robustness of the Specman-directed random-verification approach.

The ST Microcontroller Division can now seamlessly integrate newly created digital IP with existing VIPs to provide differentiated solutions for their customers. The team can start the verification process much earlier to speed projects and achieve higher levels of quality than ever before.

"Cadence solutions require ramp-up time, but the investment is really worthwhile," Auditore says. "You end up with a flow that's much more complete, integrated, and strong—that covers every aspect of digital verification."