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Samsung and Cadence

"Samsung and Cadence implemented a structured approach for the verification of Samsung's mobile application processor Exynos, as the chips grow through 150 million gates. The early results from this collaboration used Cadence Incisive Enterprise Simulator to reduce iteration time by 80-90%, enabling nightly regression for RTL simulations and two-day regression for gate-level simulations."

Byeong Min, Master of Infrastructure Design Center, System LSI Business, Samsung

The Customer

Samsung's System LSI Business develops and produces a wide range of logic products that operate and control electronic applications. Responding to the expanding mobile electronics market, this Samsung group supplies integrated multifunctional low-power semiconductor solutions. It keeps an open line of communication with customers regarding systems on chips (SoCs), image sensors, and display integrated circuit (IC) solutions in order to develop innovative products that consistently add value.

Recently the System LSI Business group launched the high-performance Exynos SoC family. These increasingly popular mobile application processors support low-power requirements and provide optimal processing power for mobile devices. In the area of CMOS image sensors (CIS), for example, Samsung maintains strong growth by supplying high-pixel products for mobile devices and expanding the application of these products to digital still cameras, webcams, and other digital devices.

In the foundry sector, Samsung has successfully introduced cutting-edge 32nm/28nm low power-consumption high-k metal-gate (HKMG) process technology for premium customer solutions. To further expand the company's growth in the smart mobile market, the System LSI Business group plans to make aggressive investments in research and development to develop competitive new products with early-to-market availability.

The Challenge

SoC verification is undergoing multiple methodology shifts in response to a single, unrelenting driver—complexity. The entire engineering team experiences SoC complexity, but verification is a different story. When the design size doubles, the verification

Business Challenge

- Reduce regression turnaround time (TAT) from five days to one day for register-transfer level (RTL), and from five days to two days for gate-level simulation (GLS)

Design Challenges

- The application processor system on chip (SoC) would quickly grow to 150 million gates and beyond
- Logic simulation runtime takes longer and consumes more memory with each design generation

Cadence Solutions

- Incisive Enterprise Simulator
- Incisive SimVision
- Incisive Enterprise Manager
- Incisive Verification IP (VIP)
- Accellera's Universal Verification Methodology (UVM)

Results

- Reduced RTL regression time by 80% and GLS by 60%
- Achieved 1.5x speed increase for Standard Delay Format (SDF) GLS and 2.2x speed increase for zero-delay GLS
- Reduced long-running RTL simulation time from 100 hours to 4 hours
- Reduced number of simulation builds from 315 to 20, saving 96% of disk space and 42% of total regression runtime

task grows exponentially because it operates in the state-space of the storage elements (both hardware and software) within the design.

Figure 1 is a block diagram of Samsung's mobile application processor Exynos, in which the complexity of the SoC verification task may not be initially apparent. Conventionally, each intellectual property (IP) block is verified, followed by each subsystem, and then the full SoC is integrated for connectivity verification. At the scale of the chip in Figure 1, the ability to execute verification is failing in two dimensions—the ability to execute a traditional simulator use model and the ability to use a monolithic verification methodology.

On the simulator side, the complexity consumes more memory and more runtime. For the SoC in Figure 1, there are 15 RTL subsystems, each between 7 million and 35 million gate-equivalent in size.

The SoC testbench is about 1 million lines of code written with IEEE 1800 SystemVerilog and IEEE 1647 e languages, including thousands of tests that address specific verification targets. Each RTL test runs between two and eight hours with a full RTL regression consuming two to three days.

At the gate level, due to the nature of tests, the memory consumption becomes larger, such as 128GB for built-in self test (BIST) and 55GB for automatic test pattern generation (ATPG) test architectures. Similar to RTL verification, the full gate-level regression is four to five days.

The big challenge for growing SoC verification is to reduce the regression time to fit in the scheduled window and optimize memory usage to allow better use of the computer farm while improving productivity. The turnaround time (TAT) to elaborate the simulation, run it, and then debug, was much too long to keep the Samsung design and verification teams operating at peak efficiency.

On the methodology side, the complexity means higher reliance on multiple teams delivering IP and verification IP (VIP) from both internal and third-party sources. While methodology consistency is the goal, it may not be possible to strictly enforce it. This increases the need for interoperable solutions.

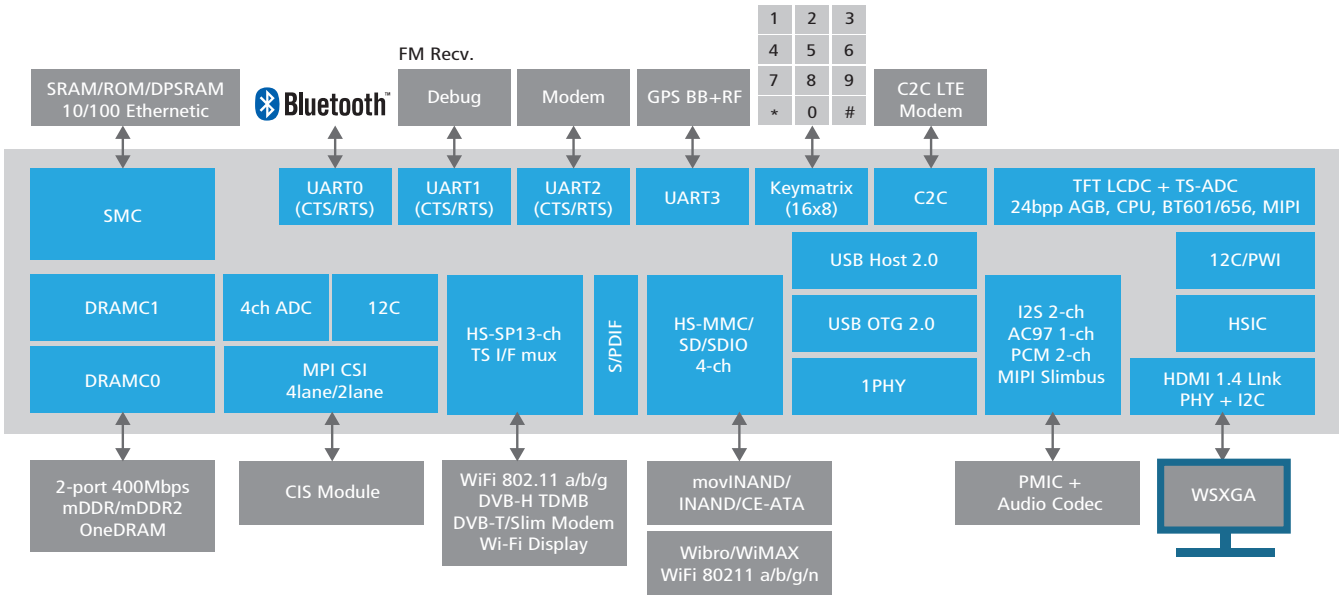

Figure 1: Application processor SoC block diagram

The Solution

Together, Samsung and Cadence developed tool and methodology solutions to enable the successful verification of Samsung's application processor SoCs.

"Samsung and Cadence implemented a structured approach for the verification of Samsung's mobile application processor Exynos, as the chips grow through 150 million gates," says Byeong Min, Master of Infrastructure Design Center, System LSI Business, Samsung. "The early results from this collaboration used Cadence® Incisive® Enterprise Simulator to reduce iteration time by 80-90% enabling nightly regression for RTL simulations and two-day regression for gate-level simulations."

"At a higher level, this involves managing the SoC verification from a plan and collecting metrics from the regression to determine progress against the plan," Min continues. "At a deeper level, it means establishing multi-language reuse methodologies and optimizing the TAT to speed both test development and debug."

A plan-based SoC verification flow is critical to assure the coverage goals are met most efficiently. Figure 2 shows the overall approach used by Samsung's application processor team. It starts with a verification plan at the SoC level, which consists primarily of Samsung's subsystems and also includes third-party IP. The combined suite of IP uses e, SystemVerilog, and Verilog languages with the top-level testbench implemented in Universal Verification Methodology (UVM) SystemVerilog. The verification plan drives the development of subsystem tests and the configuration of subsystem/IP.

The Samsung team uses Cadence Incisive Verification Manager to distribute the regression tests into the computing farm and then uses the resulting collection of coverage metrics to validate the effectiveness of the test suite. Based on the collected data, the tool directs the team to add tests in the areas of greatest overall impact.

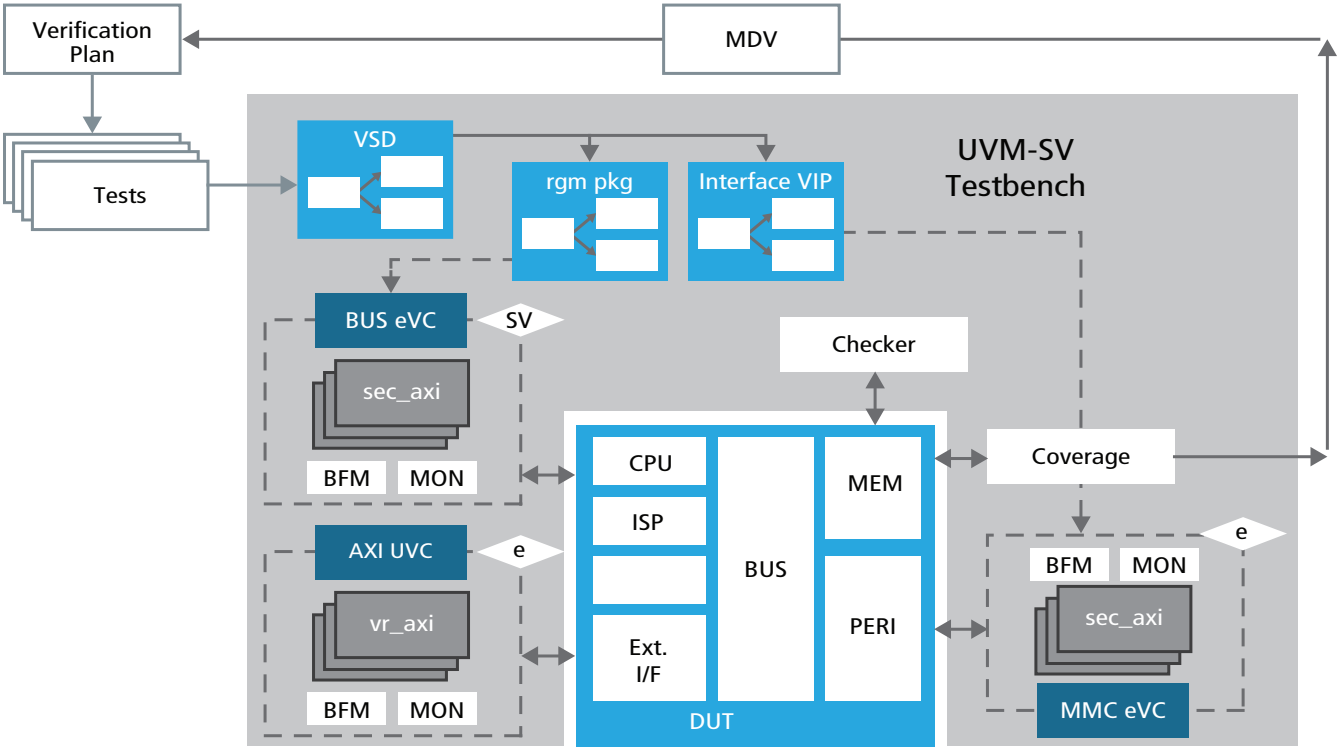

Figure 2: SoC verification environment

As mentioned earlier, the biggest simulation challenges were at the next level in the detailed regression flow. Initially, each test in the regression plan had its own simulation image, or snapshot, and this process created 315 RTL snapshots that each consumed 3GB to 5GB of disk space. This approach was largely impacting disk-space usage and the time to generate snapshots. At gate level, the impact was a very long elaboration time—more than three to four hours.

The solution was to improve the regression flow by applying the incremental elaboration feature of Incisive Enterprise Simulator for both the RTL and gate level.

At RTL, the solution generates a smaller number of common configurations with the advantage of using only 20 snapshots (called primary snapshot, one for each specific configuration). Each primary snapshot is in the range of 3GB to 5GB, but the total disk space is reduced because each individual test among the 315 in the regression suite only adds a small incremental snapshot to the primaries. Figure 3 shows the details of this flow. This saves 96% of disk space and reduces regression time up to 42%. With some specific tests the advantage is even greater, with 98% faster TAT, shortening the process from 14 minutes to 14 seconds as shown in Figure 4.

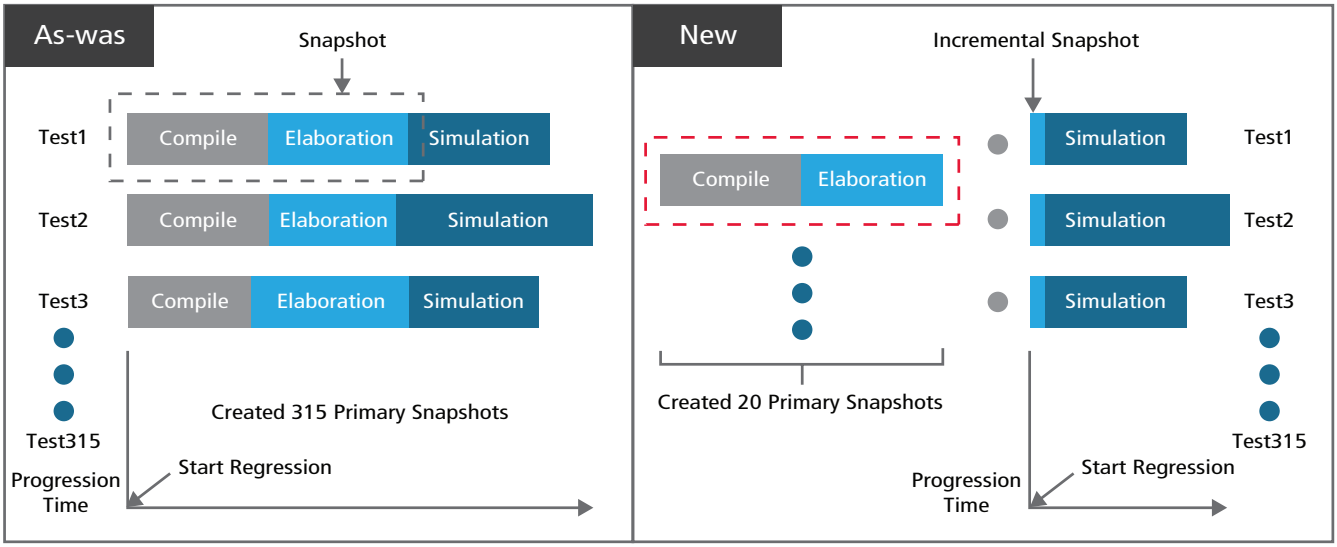

Figure 3: Improved SoC regression flow

Tests	Types	Single Elaboration Time (A)	Incremental Elaboration Time (B)	Time Reduced (A-B)/A (%)
I2C	RTL	840s	14.2s	98%
ATPG	Gate	8054s	1318s	84%
BIST	Gate	12170s	675s	95%

Figure 4: Incremental elaboration speeds TAT

At the gate level, the Samsung team applied the concept of the primary and incremental snapshot to the design under test (DUT) and the testbench respectively, based on BIST or ATPG test architectures. The advantage is the single generation of the primary snapshot, which is traditionally time-consuming due to its complexity, and fast test suite turnaround using the incremental snapshot.

"Our application processor SoCs are 150 million gates and growing larger each year. Our collaboration with Cadence enabled us to reduce our RTL regression time by 80% and gate-level regression by 60%, which is important for achieving our time-to-market goals."

With incremental elaboration, Incisive Enterprise Simulator was improved to reduce peak memory and improve runtime performance. For the BIST simulations, the elaboration memory was reduced from 128GB to 80GB and the elaboration time was improved 18x while the runtime was reduced from 40 hours to 27 hours. The results for the ATPG test were similar, with elaboration memory reduced from 55GB to 38GB, elaboration time improved by 6.1x, and runtime reduced from 12 hours to 9 hours. The close collaboration between the two companies allowed the successful deployment of these techniques and methodologies for design production, improving productivity and quality of results.

Summary

Min says, "Our collaboration with Cadence enabled us to reduce our RTL regression time by 80% and gate-level regression by 60% which is important for achieving our time-to-market goals."

"Design complexity is still doubling in each generation, so more collaboration is needed," Min continues. "We're collaborating with Cadence to look for the next generation of technologies and methodologies to address future design and verification challenges, and to enable the delivery of high-quality ICs and systems."

Moving ahead Samsung is considering several technologies, including: multi-subsystem elaboration (multi-snapshot), which generalizes the solution described in this document; multi-core simulation to further improve verification efficiency; and acceleration, where an order-of-magnitude improvement is possible.

"We're also carefully watching the Accellera Systems Initiative UVM for the SoC testbench to enhance multi-language interoperability among VIP components," Min says.