

Dual 7-bit, 3GHz Digital-to-Analog Converter IP

TSMC 28HPM Process

Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The **Cadence Dual 7-bit, 3GHz DAC IP** is a dual 7-bit DAC with differential outputs. Each DAC supports sustained conversion rates of 3GHz.

The **Cadence Dual 7-bit, 3GHz DAC IP** supports both single-ended CMOS and differential Current-Mode Logic (CML) clock inputs for maximum flexibility. It also has an 8:1 input data multiplexer to reduce data bandwidth from the high conversion rate used by the DACs to a rate usable by the system logic.

The **Cadence Dual 7-bit, 3GHz DAC IP** has clean, well-defined interfaces for easy incorporation into any system-on-chip (SoC) design. A Cadence-standard Analog Test Bus is included to facilitate preproduction testing.

Implemented on the TSMC 28HPM process, the **Cadence Dual 7-bit, 3GHz DAC IP** provides a cost-effective, power-efficient solution for demanding applications. It offers SoC implementers the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs.

The **Cadence Dual 7-bit, 3GHz DAC IP** is silicon-proven, and has been extensively validated.

Cadence IP Factory offers a comprehensive IP solution that is in volume production, and has been successfully implemented in many applications.

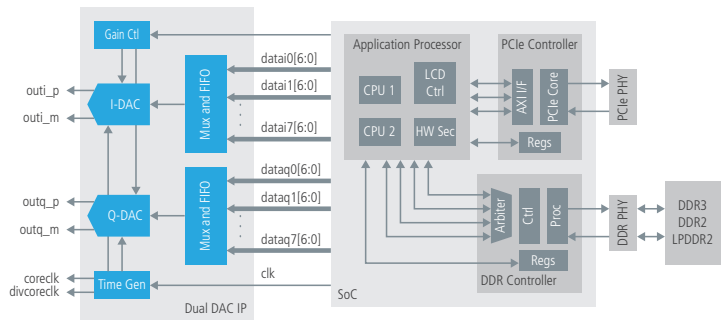


Figure 1: Example System-Level Block Diagram

Key Features

- Dual 7-bit, 3GHz Digital-to-Analog Converters
- Low power (typ. 44mW at 3GHz)
- Programmable 6-bit gain control
- Analog test bus for preproduction testing
- Small footprint
- Multi-level power-down mode
- Dynamic power-saving features
- 8:1 input data multiplexer

Product Details

The **Cadence Dual 7-bit, 3GHz DAC IP** is a hard macro for the TSMC 28HPM process. Integrated low-capacitance I/O pads are available as an option.

The **Cadence Dual 7-bit, 3GHz DAC IP** supports conversion rates up to 3GHz. It is designed to easily integrate into any SoC design with clean, well-defined interfaces, and separate analog (1.8V and 0.9V) and digital (0.9V) domains.

FIFO Block

Each DAC in the **Cadence Dual 7-bit, 3GHz DAC IP** contains a FIFO Block to reduce noise on the output due to changes on the data inputs.

DAC and Timing Generator

Each DAC uses a current-steering architecture where the full scale output current can be configured by the user. External components, or built-in resistors, can be used to convert the output current to a voltage.

The Timing Generator allows selection between a single-ended CMOS clock, or a differential CML clock. Core and divided core clock outputs are also provided.

DAC Biasing and Gain Control

The **Cadence Dual 7-bit, 3GHz DAC IP** includes an internal bias resistor, and external bias input for setting the maximum full-scale output current of the DACs.

The internal bias resistor allows the DACs to drive the internal load resistors. Using the internal bias resistor enables a full-scale output voltage independent of resistor corner variations when the internal load resistors are chosen.

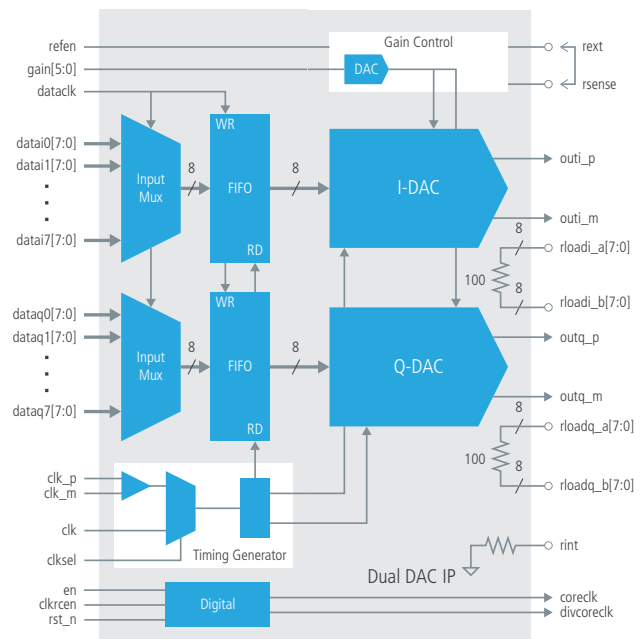


Figure 2: IP-Level Block Diagram

The **Cadence Dual 7-bit, 3GHz DAC IP** also includes a 64 step (6-bit) programmable gain control for dynamically adjusting the full-scale output of the DACs.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of DAC IP to meet your design requirements.

With 10+ years of experience and 400+ successful designs in process nodes ranging from 180nm to 22nm, Cadence IP has been proven in everything from low-power MP3 players to leading edge supercomputers.

For more information, visit ip.cadence.com

Benefits

- High conversion rate to digitize wide-bandwidth signals
- Small footprint
- Low-power—power can be dynamically reduced
- Straightforward integration
- 8:1 input data multiplexer—reduces system clock rate requirements

Related Products

- Dual 7-bit, 3GSps ADC IP, TSMC 28HPM

Deliverables

- Standard integration views—timing, physical views, LEF, DRC, LVS, ANT
- GDSII layout
- Complete documentation customized to your specific configuration

Available Products

- Dual 7-bit, 3GHz DAC IP, TSMC 28HPM

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The IP described in this document may only be taped out and manufactured at a TSMC approved manufacturing facility. Any IC developed from this IP Core must include layer 63 and any other tagging layers (including all tracking tags) as required by TSMC.

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V2.2 09/14, IP no. IP9932