

Dual 7-bit, 3GSps Analog-to-Digital Converter IP

TSMC 28HPM Process

Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The **Cadence Dual 7-bit, 3GSps ADC IP** is a dual 7-bit ADC with differential inputs. Each ADC supports sustained conversion rates of 3GSps.

The **Cadence Dual 7-bit, 3GSps ADC IP** supports both single-ended CMOS and differential Current-Mode Logic (CML) clock inputs for maximum flexibility. It also has an 8:1 data multiplexer to reduce data bandwidth from the high conversion rate used by the ADCs to a rate usable by the system logic.

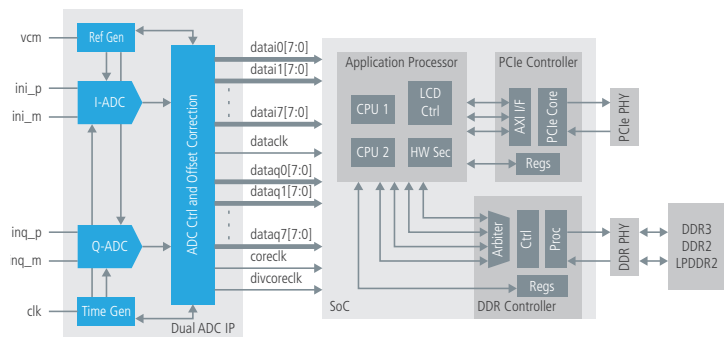


Figure 1: Example System-Level Block Diagram

The **Cadence Dual 7-bit, 3GSps ADC IP** has clean, well-defined interfaces for easy incorporation into any analog front-end (AFE) or system-on-chip (SoC) design. A Cadence-standard Analog Test Bus is included to facilitate preproduction testing.

Implemented on the TSMC 28HPM process, the **Cadence Dual 7-bit, 3GSps ADC IP** provides a cost-effective, power-efficient solution for demanding applications. It offers AFE implementers the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs.

The **Cadence Dual 7-bit, 3GSps ADC IP** is silicon-proven, and has been extensively validated.

Cadence IP Factory offers a comprehensive IP solution that is in volume production, and has been successfully implemented in many applications.

Key Features

- Dual 7-bit, 3GSps Analog-to-Digital Converters
- Low power (typ. 162mW at 3GHz)
- Internal Reference Generator
- Analog test bus for preproduction testing
- Small footprint
- Multi-level power-down mode
- Dynamic power-saving features
- 8:1 data multiplexer

Product Details

The **Cadence Dual 7-bit, 3GSps ADC IP** is a hard macro for the TSMC 28HPM process. Integrated low-capacitance I/O pads are available as an option.

The **Cadence Dual 7-bit, 3GSps ADC IP** supports conversion rates up to 3GSps. It is designed to easily integrate into any AFE or SoC design with clean, well-defined interfaces, and separate analog (1.8V and 0.9V) and digital (0.9V) domains.

Master Sample-and-Hold Block

Each ADC in the **Cadence Dual 7-bit, 3GSps ADC IP** contains a Master Sample-and-Hold (S/H) Block with high-impedance differential inputs. The differential inputs help reduce coupled noise and improve conversion accuracy.

SAR Slices

Each ADC also contains eight parallel successive approximation register (SAR) slices. Each SAR Slice converts the output of the Master S/H Block to a 7-bit word, which is passed to the ADC Control and Offset Correction Block for processing.

ADC Control and Offset Correction Block

The ADC Control and Offset Correction Block manages the internal Reference and Timing Generators as well as the individual ADCs. It also has an Offset Correction feature that can remove some offset errors. The Offset Correction feature can be bypassed for sensitive measurement and debugging purposes.

Reference and Timing Generators

The **Cadence Dual 7-bit, 3GSps ADC IP** includes a bandgap reference and all required biasing amplifiers. The bias circuitry can be varied from its nominal set point by a digital control bus to

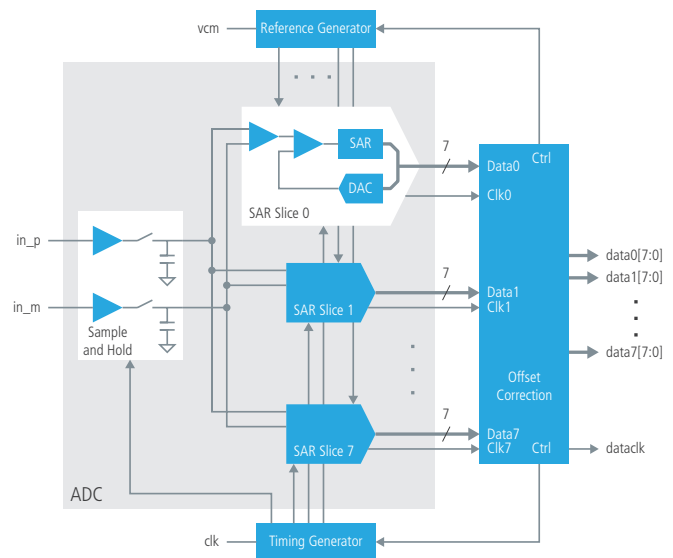


Figure 2: Single ADC IP-Level Block Diagram

optimize power consumption. All internal reference voltages and bias currents are derived from the bandgap reference.

The **Cadence Dual 7-bit, 3GSps ADC IP** also includes a programmable timing generator for adjusting sample rate to the bandwidth and power requirements of particular applications.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of ADC IP to meet your design requirements.

With 10+ years of experience and 400+ successful designs in process nodes ranging from 180nm to 22nm, Cadence IP has been proven in everything from low-power MP3 players to leading edge supercomputers.

For more information, visit ip.cadence.com

Benefits

- High conversion rate to digitize wide-bandwidth signals
- Small footprint
- Low-power—power can be dynamically reduced
- Straightforward integration
- Self-contained reference generator—no external components needed
- High-impedance input buffer
- 8:1 data multiplexer—reduces system clock rate requirements

Related Products

- Dual 7-bit, 3GHz DAC IP, TSMC 28HPM

Deliverables

- Standard integration views—timing, physical views, LEF, DRC, LVS, ANT
- GDSII layout
- Complete documentation customized to your specific configuration

Available Products

- Dual 7-bit, 3GSps ADC IP, TSMC 28HPM

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The IP described in this document may only be taped out and manufactured at a TSMC approved manufacturing facility. Any IC developed from this IP Core must include layer 63 and any other tagging layers (including all tracking tags) as required by TSMC.

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