Design IP Brochure

Device Controller IP for USB 3.0

Overview

As the Universal Serial Bus (USB) standard continues to be the common connectivity solution for both established and new, emerging types of consumer devices, the need for a robust and industry proven USB IP from a trusted provider is spreading to new markets and applications.

Certified for compliance with the USB 3.1 Gen 1 (USB 3.0) specification, Revision 1.0, the Cadence® Device Controller IP for USB 3.0 leverages deployment in numerous applications and offers to customers reliable and competitive product for all peripheral devices that make use of a USB connection.

The target applications for the Cadence USB Device Controller IP include thumb drives, SSDs, HD video cameras and other PC peripherals. Thanks to configurable system interface and endpoint space, the controller can be customized to fit single or multiple applications within an SoC.

The Device Controller IP can be delivered with either low-level or GPL Linux driver to ease integration into the target application. When integrated with the Cadence USB 3.0 Type-C™ PHY IP, the Device Controller IP provides a complete solution for the next generation of USB applications.

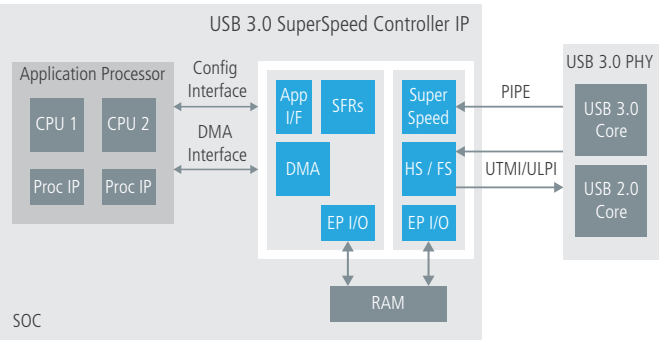

Figure 1: Example System-Level Block Diagram

Benefits

- **Complete hardware and software solution—less time spent on application development**
- **Power and clock gating enable substantial power savings**
- **Industry-standard interfaces—simple system integration**

Key Features

- Supports SuperSpeed (5Gbps), High-Speed (480Mbps), and Full-Speed (12Mbps) operation
- DMA Engine with 32- or 64-bit AXI or AHB master interface
- Certified compliance with USB 3.0 specification
- 8-, 16-, or 32-bit AHB or APB slave interface
- Up to 15 IN and 15 OUT configurable endpoints
- Supports all types of USB transfers
- Configurable PIPE 3.0 (SuperSpeed) and UTMI/ULPI (High-Speed and Full-Speed) PHY interfaces
- Full Link Power Management (U0, U1, U2 and U3) with LFPS support
- Power and clock gating support
- Compatible with the Cadence Design IP for USB 3.0 Type-C PHY

Product Details

The following sections describe the major blocks and functions of the Device Controller IP.

SuperSpeed Controller

The SuperSpeed controller implements the USB 3.0 protocol for peripheral devices. Functions are distributed among link layer and protocol layer modules, which allows the Device Controller IP to reach maximum transfer speeds of almost 98% of the theoretical maximum value.

High-Speed and Full-Speed Controller

The high-speed and full-speed controller implements the USB 2.0 protocol for peripheral devices. Data transactions, suspend and resume behavior, and interrupt generation are all handled by the high-speed and full-speed controller.

DMA Engine

The DMA engine supports scatter-gather data transfers between endpoint buffers and external memory. The host initializes a DMA transfer by writing to the DMA special function registers.

The DMA engine supports both little- and big-endian transfers.

Endpoint Logic

The Endpoint Logic generates control signals for one synchronous, single-port RAM component, which is used for both IN and OUT endpoints. RAM size is fully configurable for the number, size, and buffering requirements of endpoints.

Control transfers are handled through a dedicated IN/OUT endpoint pair with a 512 byte (64 byte for Full-Speed and High-Speed) buffer.

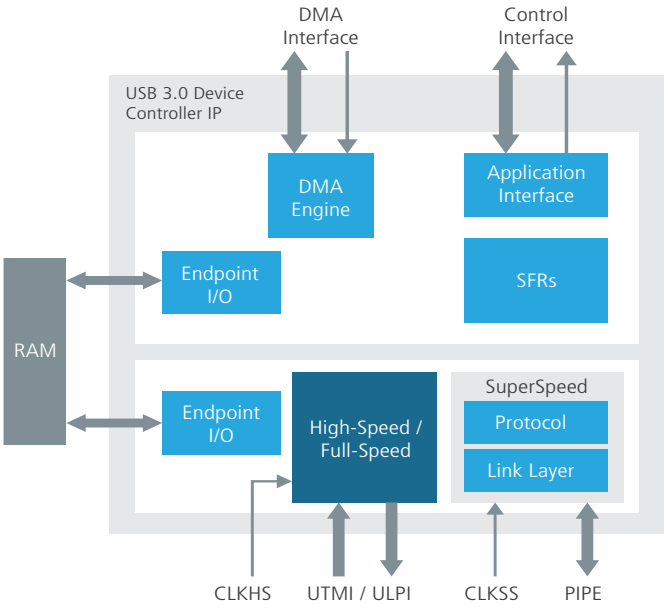

Figure 2: IP-Level Block Diagram

PHY Interface

The Device Controller IP connects to the IP for USB 3.0 PHY (SuperSpeed only) through a configurable 8-, 16-, or 32-bit PIPE 3.0 interface, and the IP for USB 2.0 PHY (High-Speed and Full-Speed) through an 8- or 16-bit UTMI or 8-bit ULPI interface.

Application Interface

The Device Controller IP supports an 8-, 16- or 32-bit AHB or APB slave interface for configuration and SFR access. Access to the DMA Engine is through a 32 or 64-bit AXI or AHB master interface.

Availability

The Device Controller IP is available with configurations below and supports the following protocols:

Protocol	Speed
USB 3.0	5 Gbps
USB 2.0	480Mbps

Related Products

- Cadence Verification IP for USB Protocols
- Cadence PHY IP for USB 3.0
- Cadence PHY IP for USB 3.0 Type-C
- Cadence Design IP for USB Type-C Port Controller

Deliverables

- Synthesizable RTL
- Testbench
- Synthesis and simulation support files
- Documentation

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