Design IP Brochure

Manager Controller IP for MIPI SLIMbus

Overview

Today's leading-edge mobile devices provide increasingly integrated functionality that enables growing volumes of audio and video, more ways to control and interact, and longer battery life. The MIPI® Alliance defines semiconductor standards for mobile devices that support growing complexity and reduced device form factor.

The Cadence® IP Family with quality products for MIPI Protocols, such as Serial Low-power Inter-chip Media Bus (SLIMbus®), delivers area-optimized interface IP with the low power and high performance required for today's leading-edge devices. One member of this family is the Cadence Manager Controller IP for MIPI SLIMbus providing low-cost, low-power connectivity for audio data transport and control.

Developed by experienced teams with industry-leading domain expertise and extensively validated with multiple hardware platforms, the Controller IP is engineered to quickly and easily integrate with other MIPI compliant IP.

The Controller IP is part of the comprehensive Cadence Design IP portfolio comprised of Interface, memory, analog, and system and peripheral IP.

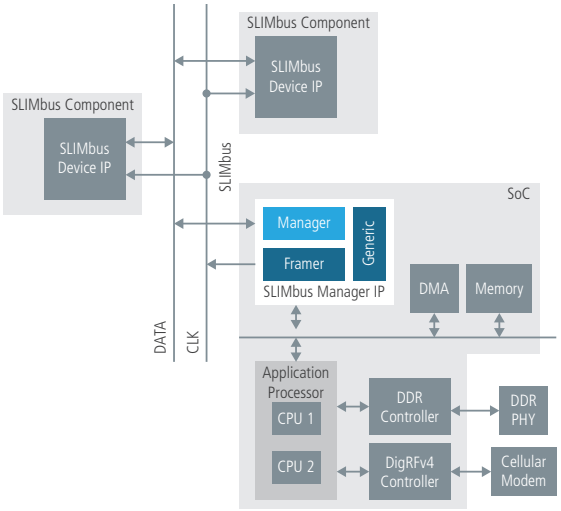

Figure 1: Example System-Level Block Diagram

Benefits

- **Full featured and highly configurable IP core that is area-optimized for each application**
- **Complete solution–complementary master/slave IP**
- **Fully verified on an FPG**

Key Features

- Up to 64 Data Ports and one Control Port supported by generic device
- Supports all core, optional, and Device Class-specific Information Elements
- 32-bit ARM® AMBA® AHB slave interface for configuration and control
- Automatic Presence Rate generation
- Support for external DMA controller to ensure efficient data transmission
- Complies with MIPI Alliance Specification for SLIMbus v1.1
- Supports all Core Messages—compatibility with other SLIMbus components and seamless message exchange
- Optional Framer and Generic Device Class support

Product Details

Compliant with SLIMbus version 1.1, the Controller IP implements Interface, Framer, Manager, and generic Device Classes with up to 64 programmable Data Ports.

The Controller IP is a synchronous, latch-free design built on a highly-configurable and scalable modular architecture to enable seamless adoption for any user application. It supports the most advanced SLIMbus features, including dynamic bus reconfiguration, multiple, simultaneous, independent data transmissions, and power consumption optimization. The optional Framer Device supports additional features such as Bus Reset, Clock Pause, Phasing Signal, and Framer Handover.

Interface Device

The Interface Device Class is implemented by such subcomponents as Receiver, Transmitter, Output Controller, and Interface Message Decoder.

The Receiver performs frame, superframe, and message synchronization. Two FSMs constitute its core–one responsible for booting process control and component synchronization, and the other handling message reception and tracking.

Shared by all internal devices, the Transmitter contains FSM and control circuits that ensure message transmission and generate data to be transmitted in the next Message Channel slot.

As the last transmit step, the Output Controller drives the SLIMbus output data port according to the Transmitter control signals and the cell number in the slot.

Generic Device

The Generic Device supports a Control Port and up to 64 Data Ports.

The Data Ports are accessible either through AHB or through a direct interface, with DMA functionality supported in both these modes. Each Data Port can be configured as a data source or sink, depending on the data channel configuration.

The IP implements the option of automatic generation of valid and invalid samples sequence according to the selected Presence

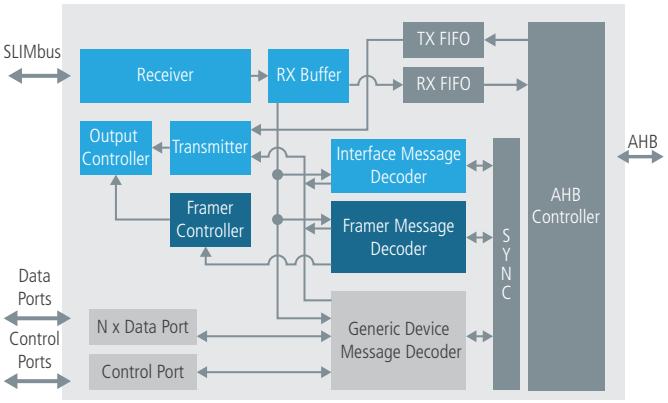

Figure 2: IP-Level Block Diagram

Rate and actual SLIMbus configuration, which enables the flow control to be done solely by the IP.

The Control Port is responsible for generation of read, write, clear, read-and-write, and read-and-clear transactions at the Control Port interface, a parallel, synchronous, read-write, SRAM interface.

Framer Device

Framer Controller and Framer Message Decoder subcomponents constitute the Framer Device.

Responsible for generating the SLIMbus clock and SLIMbus framing data, the Frame Controller implements various Framer Class functionalities, including framer booting and handover processes, SLIMbus shutdown and reset, as well as SLIMbus pausing for an indefinite number of cycles, just to list a few.

Manager Device

The Manager Device implements the Active Manager Functionality and provides the ability to transmit and receive SLIMbus messages by the software. Additionally, the IP implements the Sniffer mode by means of which all message traffic is recorded. The AHB subcomponent contains all SLIMbus Manager control and status registers accessible by CPU through AHB and is responsible for controlling AHB read and write accesses to the IP.

Related Products

- Cadence Device Controller IP for MIPI SLIMbus

Deliverables

- Clean, readable, synthesizable Verilog RTL
- Synthesis and STA scripts
- Documentation—implementation specification, user guide
- Sample Verification testbench with integrated BFM and monitors

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