

# Device Controller IP for MIPI SLIMbus

## Overview

Today's leading-edge mobile devices provide increasingly integrated functionality that enables growing volumes of audio and video, more ways to control and interact, and longer battery life. The MIPI® Alliance defines semiconductor standards for mobile devices that support growing complexity and reduced device form factor.

The Cadence® IP Family with quality products for MIPI Protocols, such as Serial Low-power Inter-chip Media Bus (SLIMbus®), delivers area-optimized interface IP with the low power and high performance required for today's leading-edge devices. One member of this family is the Cadence Device Controller IP for MIPI SLIMbus providing low-cost, low-power connectivity for audio data transport and control.

Developed by experienced teams with industry-leading domain expertise and extensively validated with multiple hardware platforms, the Controller IP is engineered to quickly and easily integrate with other MIPI compliant IP.

The Controller IP is part of the comprehensive Cadence Design IP portfolio comprised of Interface, memory, analog, and system and peripheral IP.

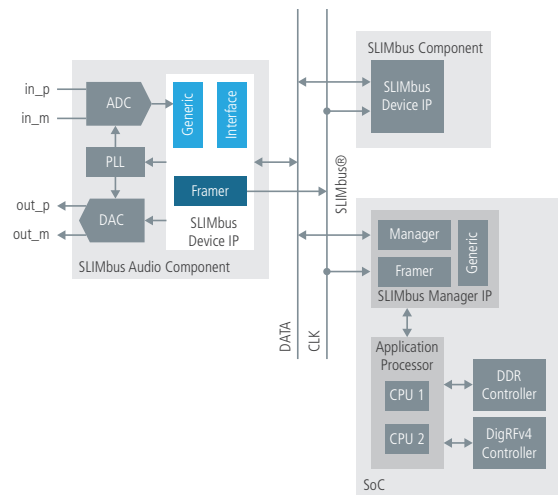


Figure 1: Example System-Level Block Diagram

## Benefits

- Full featured and highly configurable IP core that is area-optimized for each application
- Complete solution—complementary master/slave IP
- Fully verified on an FPGA

## Key Features

- Up to 64 Data Ports and one Control Port supported by generic device
- Extensive configurability options
- Control Port for control communication (for both User Value and Information Elements)
- Automatic bus detach/attach function
- Supports all Core Messages—compatibility with other SLIMbus components and seamless message exchange
- Compact size, with smallest implementation of less than 10k gates
- Complies with MIPI Alliance Specification for SLIMbus v1.1
- Supports Isochronous, Pushed and Pulled protocols

## Product Details

Compliant with MIPI Alliance Specification for SLIMbus version 1.1, the Controller IP implements the Generic Device Class with up to 64 programmable Data Ports, the Interface Device Class, and optionally, the Framer Device Class.

The Controller IP is a compact design (less than 10k gates in its smallest implementation) that is ideally suited for low-cost audio sources and sinks such as digital microphones and speakers. All devices within the Controller IP share a common receiver and transmitter, simplifying connection to the SLIMbus.

The Controller IP is a synchronous, latch-free design built on a highly configurable and scalable modular architecture to enable seamless adoption for any user application. It supports most advanced SLIMbus features, including dynamic bus reconfiguration and power consumption optimization.

## Devices

Each device (interface, generic, and optional framer) supports all core messages for that particular device class. Automatic REPLY and REPORT Messages are generated, allowing the Controller IP to operate without an external controller. Optional REPORT Message generation can be disabled.

Devices also support all core and device class-specific (mandatory and optional) information and value elements, as well as user information and value elements. The enumeration address for each device can be configured independently.

## Generic Device

The generic device supports up to 64 data ports and one control port. Each data port can be configured as a data source or sink, depending on the data channel configuration. Data width can be

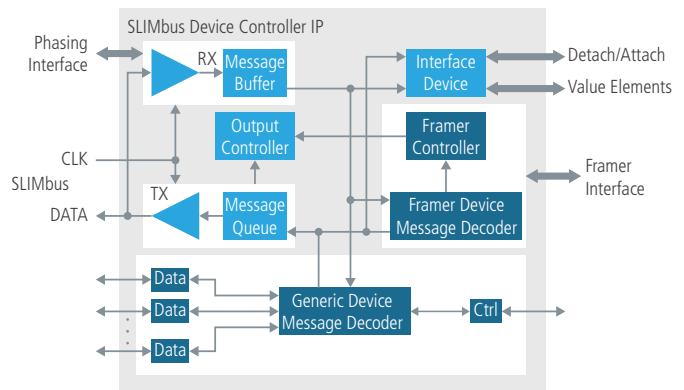


Figure 2: IP-Level Block Diagram

configured individually for each data port. Support for presence rates and transport protocols can be configured to meet specific system requirements. The generic device can support up to 64 simultaneous, independent data streams.

The control port provides a convenient interface for exchanging information with an external device. Implemented as a value element, the control port uses value element messages for read and write transactions.

## Framer Device

Compliant with MIPI Alliance Specification for SLIMbus version 1.1, the Controller IP implements the Generic Device Class with up to 64 programmable Data Ports, the Interface Device Class, and optionally, the Framer Device Class.

## Related Products

- Cadence Manager Controller IP for MIPI SLIMbus

## Deliverables

- Clean, readable, synthesizable Verilog RTL
- Synthesis and STA scripts
- Documentation—integration and user guide, release notes
- Sample Verification testbench with integrated BFM and monitors
- Optional FPGA evaluation system
- Optional EDIF netlist for FPGA and low volume production

For more information, visit [ip.cadence.com](http://ip.cadence.com)



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