Overview

Today's leading edge mobile devices contain increasingly integrated functionality that enables growing volumes of content and video, more ways to control and interact, and longer battery life. The Cadence® IP for MIPI protocols with the necessary low power and high performance, is leading the way towards MIPI® Alliance interface specifications for mobile devices that support growing complexity and reduce device form factor.

Developed by experienced teams with industry-leading domain expertise and extensively validated by multiple hardware platforms, the Cadence Receiver Controller IP for MIPI Camera Serial Interface 2 (CSI-2SM) is an all-digital design that provides a cost effective, low-power solution for demanding mobile applications. It also provides both serial pixel outputs for interfacing to an image signal processor (ISP) and packed data outputs for direct-to-memory applications.

The Controller IP offers system-on-chip (SoC) integrators the advanced capabilities and support that exceed requirements of high-performance designs and implementations.

Silicon-proven and shipping in high volume in multiple mobile devices, the Controller IP is engineered to quickly and easily integrate into any System-on-Chip (SoC) design, and to connect seamlessly to a Cadence, or third-party PPI-compliant D-PHY™ lane modules.

The Controller IP is part of the comprehensive Cadence Design IP portfolio comprised of Interface, Memory, Analog, and Systems and Peripherals IP.

Key Features

- Programmable Synchronization and Interrupt events
- Full MIPI CSI-2 data and byte-to-pixel conversion
- Compliant with MIPI CSI-2 v1.3
- Virtual Channel / Data type de-interleaving
- 32-bit ARM® AMBA® APB slave interface register access
- Packed, byte-to-pixel, multi pixel outputs
- Protocol error detection
- Supports all primary and secondary data formats

Benefits

- Full Featured and highly configurable IP core that is area-optimized for each application
- Complete solution—complementary master/slave IP
- Fully verified on an FPGA
Product Details

The Controller IP consists of a D-PHY selection and isolation module to interface to one D-PHY Receiver module, external register interface for configuration of the receiver IP and connected D-PHY lane modules, RX lane control module for dynamic contour of the D-PHY lane modules, CSI-2 protocol module for protocol functions, and CSI-2 Stream for providing the various data and pixel outputs in the correct format. A scalable memory interface is also available for connecting line memory to the receiver IP.

D-PHY Selection and Isolation Module

The D-PHY selection and isolation module provides clock isolation of the camera interface from the Controller IP, allowing the rest of receiver IP to operate at a clock rate different than the camera interface.

The D-PHY selection and isolation module also provides selection of different camera interfaces in multi-camera applications.

RX Lane Control Module

The RX lane control module provides configuration control for the D-PHY lane modules. For example, line termination and collision detection can be enabled or disabled, the DP and DN lines can be swapped, data coming from the lane module can be inverted, EOT symbols bypassed, etc.

CSI-2 Protocol Module

The CSI-2 protocol module handles the CSI-2 protocol stream coming from the camera interfaces and monitors traffic on the interfaces. It also performs error checking and correction, and CRC code checking, to ensure data integrity.

The CSI-2 protocol module also monitors the CSI-2 protocol stream for start-of-frame (SOF), end-of-frame (EOF), and truncated CSI-2 frames. The CSI-2 protocol module can generate interrupts for these conditions on two virtual channels, as well as generate interrupts for specific line/byte and timer counts on all virtual channels.

CSI-2 Stream

The CSI-2 Stream formats data from CSI-2 packets into RAW Bayer, RGB, YUV, and user-defined packed data formats. Individual serializer convert RAW Bayer, RGB/YUV, and user-defined formats into a serial stream suitable for an ISP.

Related Products

- Cadence Design IP for MIPI D-PHY
- Cadence Transmitter Controller IP for MIPI CSI-2

Deliverables

- Clean, readable, synthesizable Verilog RTL
- Synthesis and STA scripts
- Sample Verification test-bench with integrated BFM and monitors

For more information, visit ip.cadence.com

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