Overview

Cadence IP Factory delivers custom, synthesizable IP to support specific design requirements.

The Cadence QSGMII IP provides the logic required to integrate a quad serial gigabit media independent interface with QSGMII-modified PCS functionality into any system on chip (SoC).

Compliant with Cisco Systems’ proprietary QSGMII Specification, Revision 1.2, the Cadence QSGMII IP has several optional features to customize the interface for the specific needs of any application. Support for auto-negotiation via a modified version of the functionality defined in IEEE Standard 802.3z Clause 37 is also available.

The Cadence QSGMII IP is architected to quickly and easily integrate into any SoC, and to connect seamlessly to four Cadence, or third-party, MACs through a GMII (1G only) or MII (10/100M only) interface. Connection to the four SerDes is through a configurable 10-bit or 20-bit QSGMII.

The Cadence QSGMII IP is silicon proven, and has been extensively validated with multiple hardware platforms.

Cadence IP Factory offers a comprehensive IP solution that is in volume production, and has been successfully implemented in more than 400 applications.

Key Features

- Compliant with QSGMII Specification Revision 1.2
- GMII (1G only) or MII (10/100M only) interface to MAC
- Four independent 1Gb/s or 10/100Mb/s ports
- Configurable 10- or 20-bit SerDes interface
- 8b/10b encode/decode implemented in hardware
- Supports auto-negotiation
- Supports Energy Efficient Ethernet through LPI transport
Product Details

The Cadence QSGMII IP provides four channels of Gigabit or 10/100M Ethernet communication over a single 10-bit or 20-bit link. 1000BASE-X PCS functionality, such as 8b/10b encoding/decoding, modified in accordance with the QSGMII specification, is also provided.

MAC Interface

The Cadence QSGMII IP connects to the MACs through four GMII or MII ports. Each port can be independently configured as GMII (1G only) or MII (10/100M only). In the case of an MII port, a wrapper converts the 4-bit MII data into GMII octets in the transmit path, and from GMII octets into 4-bit MII data in the receive path. Each port in the transmit path is connected to a buffer to decouple the QSGMII clock from the GMII or MII clock.

State Machines and Port 0 K28.5 Swapper

Four TX State Machines, one for each port, prepare the data for multiplexing and set the operating mode as negotiated by the Auto-Negotiation block. Four state machines in the receive path perform the same function on receive.

The Port 0 TX State Machine also implements a K28.5 Swapper to replace K28.5 symbols in the GMII octet stream with K28.1 symbols as per the QSGMII specification.

8b/10b Encoder/Decoder

The Cadence QSGMII IP also contains an 8b/10b encoder and a 10b/8b decoder that operates in accordance with IEEE Standard 802.3 Clause 36, modified to support QSGMII. For 20-bit SerDes operation, the encoder concatenates two 10-bit encoded symbols to create a 16b/20b symbol, and the decoder splits the 20b/16b symbol into two GMII octets after decoding.

Comma Alignment and K28.1 Swapper

Comma alignment is provided by a dedicated block within the Cadence QSGMII IP. Once the stream is aligned, the data is passed to the K28.1 Swapper where the K28.1 symbols inserted by the transmit path are replaced by K28.5 symbols.

SerDes Interface

The SerDes interface on the Cadence QSGMII IP is configurable for 10-bit, 500MHz or 20-bit, 250MHz operation.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of media independent interfaces to meet your design requirements.

For more information, visit www.cadence.com/ip

Benefits

- Low Risk solutions – Silicon proven design
- Ease of Use – Customizable with easy integration
- Designed by an industry leader – Cadence is an active contributor to the 802.3 standards working groups

Related Products

- Cadence® Verification IP for Ethernet
- 1G Ethernet MAC IP (GEM)

Deliverables

- Verilog HDL
- Cadence® Encounter® RTL Compiler synthesis scripts
- User guide with full programming interface, parameterization instructions, and synthesis instructions
- Verilog testbench

Available Products

- QSGMII IP

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