Overview

Cadence IP Factory delivers custom, synthesizable IP to support specific design requirements.

The Cadence 40GBASE-R Ethernet PCS (PCSXL) IP provides the logic required to integrate a 40GBASE-R PCS into any system on chip (SoC).

Compliant with IEEE Standard 802.3ba-2010 Clause 82, the Cadence 40GBASE-R Ethernet PCS (PCSXL) IP has several optional features to customize the PCS for the specific needs of any application. Support for Forward Error Correction (IEEE 802.3ba-2010 Clause 74) is also available.

The Cadence 40GBASE-R Ethernet PCS (PCSXL) IP is architected to quickly and easily integrate into any SoC, and to connect seamlessly to a Cadence, or third-party, MAC through a XLGMII. Connection to each SerDes is through a programmable 16- or 32-bit interface.

The Cadence 40GBASE-R Ethernet PCS (PCSXL) IP is silicon proven, and has been extensively validated with multiple hardware platforms.

Cadence IP Factory offers a comprehensive IP solution that is in volume production, and has been successfully implemented in more than 400 applications.

Key Features

- Compliant with IEEE Standard 802.3ba-2010 Clause 82
- 64-bit XLGMII connection to the MAC
- Lane reordering to align received lanes with transmitted lanes
- Data scrambling on transmit path and descrambling on receive path
- Programmable PRBS31 and PRBS9 (Clause 68) test pattern generators and error checkers
- 64b/66b encoding/decoding using reduced encoding table for 40GBASE-R
- Clock tolerance compensation on receive path
- Configurable 16- or 32-bit SerDes interface
- Optional Forward Error Correction (Clause 74)
- Internal loopback modes available
Product Details

The Cadence 40GBASE-R Ethernet PCS (PCSXL) IP is designed as an on-chip PCS for connecting a 40G MAC to four 10G SerDes. It supplies all PCS functionality as well as some PMA features.

64b/66b Encoder and Decoder

The 64b/66b Encoder takes eight octets (64-bits) from the XLGMII and codes them into a single 66-bit block.

The 66b/64b Decoder takes 66-bit blocks from the Gearbox or, after FEC transcoding and error correction, from the optional FEC block, and decodes the block into eight octets.

Both the 64b/66b Encoder and 66b/64b Decoder use the reduced encoding table for 40GBASE-R.

Data Scrambler and Descrambler

The Data Scrambler uses the algorithm defined in IEEE 802.3ba-2010 Clause 82.2.5 to scramble the data after line coding.

The Data Descrambler reverses the scrambling algorithm applied by the Data Scrambler in accordance with IEEE 802.3ba-2010 Clause 82.2.15.

Gearbox and SerDes Interface

The Gearbox converts signals between the 66-bit width used by the PCS and the bit-width used by the 10G SerDes. It also distributes the 66-bit blocks to the four SerDes and inserts alignment markers on transmit. On receive, the Gearbox reorders the 66-bit blocks from the SerDes and removes the alignment markers. The SerDes interface is configurable for either a 16-bit or 32-bit width.

Test Pattern Generators

The Cadence 40GBASE-R Ethernet PCS (PCSXL) IP has built-in PRBS31 and PRBS9 (Clause 68) test pattern generators and checkers for testing the integrity of the link. A separate square wave pattern generator is also included.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of PCS to meet your design requirements.

For more information, visit www.cadence.com/ip

Benefits

- Low Risk solutions – Silicon proven design
- Ease of Use – Customizable with easy integration
- Designed by an industry leader – Cadence is an active contributor to the 802.3 standards working groups

Related Products

- Cadence® Verification IP for Ethernet
- 40GBASE-R Ethernet PCS IP (PCSCG)

Deliverables

- Verilog HDL
- Cadence® Encounter® RTL Compiler synthesis scripts
- User guide with full programming interface, parameterization instructions, and synthesis instructions
- Verilog testbench

Available Products

- 40GBASE-R PCS IP (PCSXL)