cadence®

SoC Verification Using Cadence Verification IP

An in-depth examination of SoC verification/validation approaches including Accelerated VIP

Traditional simulation-based verification time can be excessive at the subsystem, SoC, and system levels. Many companies are adopting acceleration platforms and Accelerated Verification IP (AVIP) to address this challenge. This paper explores the use of verification IP for hardware verification at the IP/subsystem, SoC, and hardware/software integration levels. It also examines how Cadence® technology enables project teams to shorten verification time and improve product quality by employing the tools and techniques best suited for each integration level.

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Introduction

As designs have grown into the 10s and even 100s of millions of gates, it has become a necessity for design and verification teams to expand the range of functional verification tools that they employ. In the 1990s and early 2000s, the majority of designs were completed using logic simulation, from the IP level all the way to chip-level verification. As system hardware and software has grown in complexity in recent years, simulation times have become excessive for many designs. Consequently, the demand for accelerated and/or emulated platforms and Accelerated Verification IP (AVIP) has increased dramatically. This paper describes the range of solutions Cadence provides to address the many needs of design and verification teams, with a spotlight on the Cadence Verification IP (VIP) Catalog, which includes AVIP to provide the most comprehensive standard-protocol verification solution.

The New System Methodology

Companies facing challenges with traditional simulation-based verification have adopted acceleration and/or virtual prototyping to reduce their overall product development cycle and to enable subsystem or full SoC verification. They use a variety of execution engines optimized for incremental, agile, and high-performance flows. This enables a variety of models to be employed, as shown in Figure 1. This paper's focus is on VIP usage for hardware verification at the IP/subsystem, SoC, and hardware/software integration levels (i.e. the three lower rows in Figure 1).

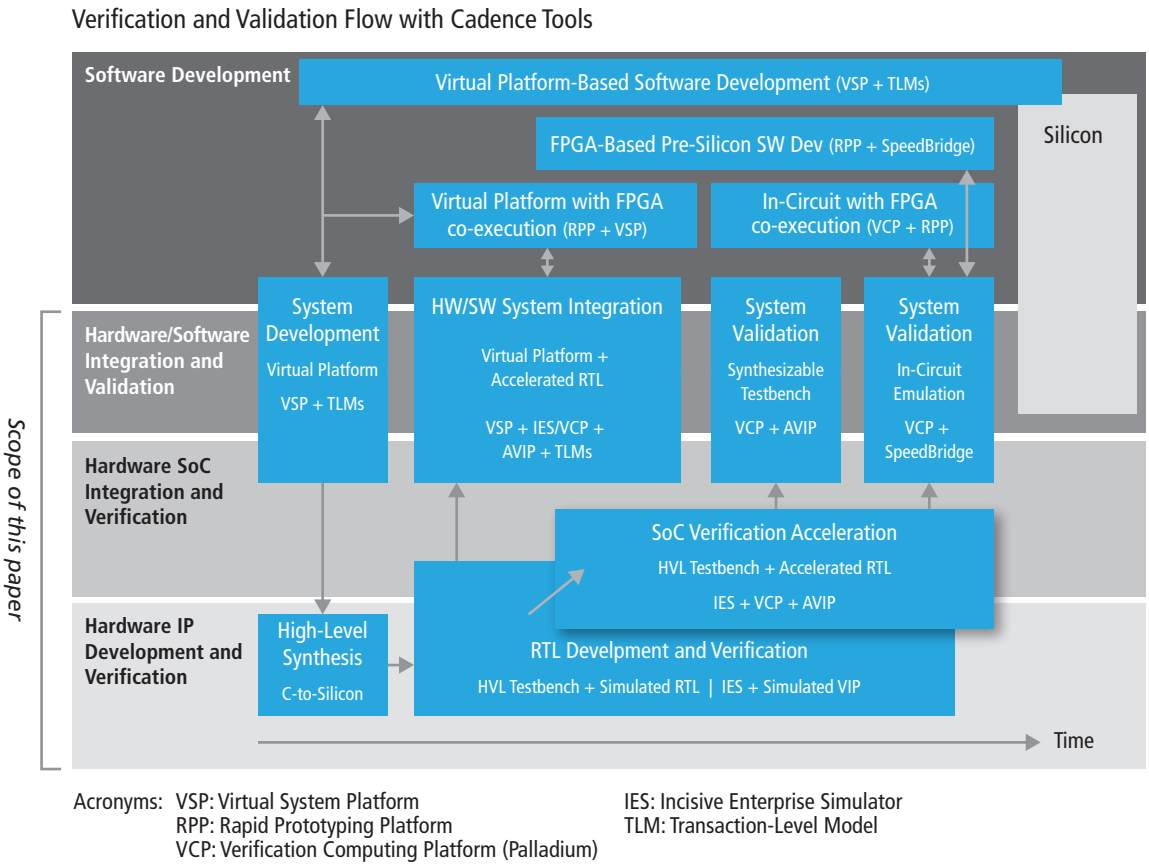

Figure 1: System development flow with mapping to Cadence verification solutions

Leading companies have also adopted a tiered system integration and verification methodology. Their best practices include setting verification goals for each integration tier and selecting the verification methods and metrics to maximize those goals. Cadence recommends the following goals and methods for each hardware-dependent integration level:

Hardware IP development and verification

- Goals: exhaustive algorithm and full protocol-compliance verification to find all corner-case bugs
- Methods: simulation with metric-driven verification employing IP-appropriate metrics, with massive constrained-random stimuli
- VIP: simulated VIP supporting full protocol-compliance verification, including a Universal Verification Methodology (UVM) user interface

Hardware subsystem/SoC verification

- Goals: verify SoC functions, the interaction between SoC blocks, and SoC performance and power
- Methods: simulation and hardware-assisted acceleration employing SoC-level–appropriate metrics, with system-level constrained-random stimuli and software use-case scenarios
- VIP: simulated and Accelerated VIP (AVIP) supporting multiple user interfaces, including the UVM for system verification and C for software development and integration

Hardware/software integration and validation

- Goals: validate full system behavior by ensuring correct software and hardware interaction; provide a software development platform; tune system power and performance
- Methods: hardware emulation and embedded (synthesizable) testbench employing software use-case scenarios

- VIP: Accelerated VIP (AVIP) supporting embedded testbench use models, and a C or transaction-level model (TLM) 2.0 user interface for externally generated stimulus or SpeedBridge® Adapters to connect to real-world stimulus

To achieve appropriate results at each integration tier, it is critical to set the right goals and use the right tools applicable at each stage. For example, performing exhaustive protocol verification at the full SoC level would result in prohibitively long execution times, even on the fastest execution engine. Conversely, by limiting the verification goals to SoC-level functions, the interaction between subsystems allows timely execution of many randomized or software-driven use-case scenarios.

A Verification IP Catalog to Meet the Growing Range of Requirements

State-of-the-art system development requires multiple design abstractions and integration levels, as well as multiple execution platforms such as simulation and hardware-assisted verification. Multiple forms of verification IP (VIP) are required to support this spectrum of abstractions and integration levels.

Cadence provides the industry's leading VIP solution with support for a broad set of protocols and deep verification capabilities, including automated protocol-compliance verification. The Cadence VIP Catalog is highly mature, having been proven on thousands of customer designs, and now supports a range of verification platforms including simulation, acceleration, and formal verification. These capabilities improve design quality while reducing overall verification time and effort.

- Cadence simulated VIP enables metric-driven verification (MDV) for exhaustive protocol verification by utilizing built-in coverage, randomization, and compliance checks. This enables design and verification teams to gauge the readiness of the block IP for subsystem or chip-level integration once protocol compliance meets the needs of the given application. The return on investment for block-level protocol-compliance verification is in the significant reduction of protocol-level issues, which will be avoided in system-level use models. Low-level protocol issues during system validation can derail hardware/software co-verification tasks and require significant iteration on the block-level IP design, leading to delays in release schedules. Simulated VIP contains a protocol core optimized to maximize coverage and simulation performance
- Cadence Accelerated Verification IP (AVIP) takes full advantage of the Palladium® XP Verification Computing Platform's architecture and speed. AVIP provides transaction-based acceleration for designs including AMBA® AXI™ and PCI Express protocols. Coupled with a high-performance testbench, AVIP dramatically accelerates SoC/system-level verification performance and throughput. AVIP utilizes a synthesizable protocol core optimized for acceleration performance
- Embedded AVIP uses the same optimized core as AVIP but executes embedded in the design, without an external testbench. Embedded AVIP provides in-circuit–level performance

Cadence simulated VIP and AVIP is UVM-compatible, allowing environment reuse between simulation and acceleration platforms. For example, users can swap simulated VIP and AVIP in a system-level testbench. Additionally, IP/block-level UVM environments that utilize Cadence simulated VIP can be reused between simulation and acceleration with minimal changes.

Unlike other EDA vendors' solutions, the Cadence VIP portfolio enables users to control the tradeoffs between verification exhaustiveness and execution performance:

- Select the best form of VIP for each testbench (simulated or accelerated)
- Select the desired level of generation coverage and checking when using AVIP with a UVM interface
- Maximize performance for software development and system validation applications using AVIP with a C interface or embedded AVIP

Testbench Impact on Acceleration Performance

Verification acceleration performance is inversely proportional to the percentage of CPU time consumed by the testbench vs. the design, when measured during simulation. For example, a verification environment in which the testbench consumes 1% of CPU cycles can be accelerated up to 100x over simulation. Testbench performance is influenced strongly by the amount of testbench activity including (but not limited to) generation, compliance checking, error injection, and coverage collection. High-performance testbenches use the minimum generation and coverage required to meet the verification goals for the intended integration stage.

Acceleration performance is also strongly related to the communication efficiency between the testbench and the emulation system. To maximize speed, transaction-based interfaces are used by all Cadence VIP and are recommended for other high-traffic interfaces crossing the testbench/design under test (DUT) boundary.

VIP Usage Recommendations

Figure 2 illustrates Cadence recommendations on how to best address verification needs at each integration step. The remainder of this paper focuses on how to apply Cadence VIP within the two verification acceleration focus areas labeled "A" and "B" in Figure 2.

		A	B	C	
		Signal-Level Testbench with Simulated VIP	Transaction-Level Testbench with AVIP	Synthesizable Testbench with Embedded AVIP	In-Circuit Emulation with SpeedBridge[1] Adapter
HW/SW Integration and Validation	Performance		50-500x (acceleration)	10,000x	10,000x
	Testbench		External C	Embedded test SW	Target device
	Generation		C-test dependent	None	None
	VIP coverage		n/a	n/a	n/a
Subsystem and SoC Integration and Verification	Performance	1x (simulation)	2-3x (sim), 50-300x (accel)		
	Testbench	UVM	UVM		
	Generation	System level	System level		
	VIP coverage	Optimized core, UVM layer	UVM layer		
Block and IP-Level Verification	Performance	1x (simulation)			
	Testbench	UVM			
	Generation	IP level			
	VIP coverage	Optimized core, UVM layer			

1. SpeedBridge rate adapters interface the Palladium platform to external systems, networks, and test equipment. This enables teams to emulate the design with real application requirements such as booting the operating system or displaying graphics and video.

Figure 2: VIP application by integration stages

Column A articulates the primary recommended usage for simulated VIP. The application is IP-level and block-level or SoC-level verification, where a high level of compliance checking across a broad set of protocol-specific scenarios is required.

As more blocks and subsystems are integrated into a given simulation environment, the complexity and size of the design negatively impact the project team's efficiency at validating long system-level test cases. Depending on the overall design complexity and test characteristics, simulation performance may not enable all project needs for subsystem verification tasks.

This verification performance gap is best addressed through a combination of high-performance, transaction-level testbenches and Accelerated VIP as shown in column B. This use model is known as verification acceleration.

Software development and software-driven system validation use models require even higher levels of performance. These use models are addressed using synthesizable testbenches and in-circuit emulation, depicted in column C.

Implementing the use models depicted in Figure 2 requires verification platforms that support the following capabilities:

- RTL simulation with advanced metric-driven verification
- Acceleration of signal-based verification environments (signal-based acceleration)
- Acceleration of transaction-based verification environments (transaction-based acceleration)
- Synthesizable testbench supporting software-driven use-case tests (embedded testbench)
- In-circuit emulation (ICE)

Cadence verification products, including Incisive® Enterprise Simulator, Palladium XP Verification Computing Platform, VIP Catalog, and SpeedBridge Adapters, are designed to support the execution of and the flows among the aforementioned use models.

Cadence VIP Architecture

Cadence VIP is architected to address several key top-level requirements:

- Enable maximum reuse between simulation and acceleration
- Support the UVM and multiple languages
- Provide the capabilities needed to best support each use model
- Optimize performance on each platform

Cadence simulated VIP architecture

Simulated VIP provides a UVM user interface along with an optimized simulation core to deliver advanced verification capabilities for block-level protocol compliance and subsystem verification.

Figure 3 shows the VIP architecture of a UVM-compliant user interface for both SystemVerilog and e languages. It includes agents, tests, sequences, complete protocol compliance checking, customizable configuration, and a coverage model to efficiently collect and report coverage. The architecture also provides a methodology-independent interface: an alternative or supplemental API to the UVM, enabling use with multi-language and application-specific customer verification environments. Finally, a signal-level interface is provided to connect directly to the user's DUT physical interface.

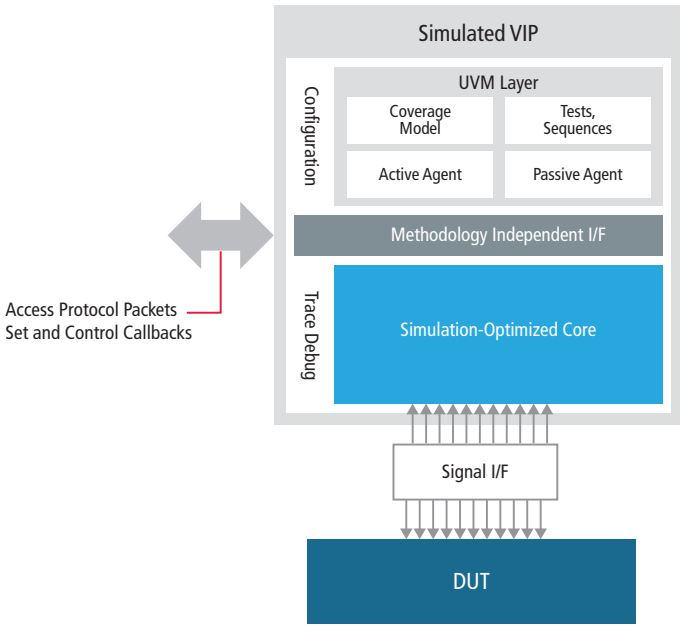

Figure 3: Simulated VIP architecture

The UVM layer defines the use of constrained randomization to ease the generation of a full set of protocol scenarios to verify compliance with a given protocol standard. The UVM user interface provides physical fields and virtual fields, both of which users can also randomize or set specifically. Physical fields are directly related to signals defined by the standard and are associated directly with access to the DUT. Examples of physical fields for these protocols include address, kinds of data items, length, and CRC.

Virtual fields are defined to enable the user to control and access verification capabilities. The VIP's optimized core utilizes the virtual fields to adjust the execution of its state machines, which drive the signals of the physical interface. The coverage model (in the UVM layer and in the simulation-optimized core) collects coverage that can be leveraged and managed using Incisive Enterprise Manager.

Cadence VIP provides a robust test suite to expedite high levels of protocol compliance:

- A broad set of sequences that stimulate the DUT
- A set of DUT configurations (modes) that provide required responses
- A coverage model for the standard specification
- Constraints
- A data item that contains physical and virtual fields
- An optimized core that can handle the virtual fields to create special verification scenarios

The constraints directly impact the sequences that are run using the provided data items. The data item and optimized core are part of the baseline VIP architecture. Additionally, users can configure which sequences should be run based on the compliance requirements of their design (directly related to the provided sequences and constraints). Finally, the VIP can provide a verification plan (vPlan) based on the protocol standard's outline. The collected coverage is reported in the appropriate sections of the vPlan using vManager.

Cadence AVIP architecture

The architecture of Cadence Accelerated VIP was designed to support the three primary goals of system-level verification: (1) high performance and throughput; (2) environment reusability between simulation and acceleration; and (3) support for accelerated metric-driven environments.

The AVIP architecture enables multiple interfaces and use models including UVM, C, and embedded. It is important to understand that AVIP architecture uses same UVM layer as employed in the simulated VIP. The three architectural implementations corresponding to the UVM, C, and embedded use models are depicted in Figure 4.

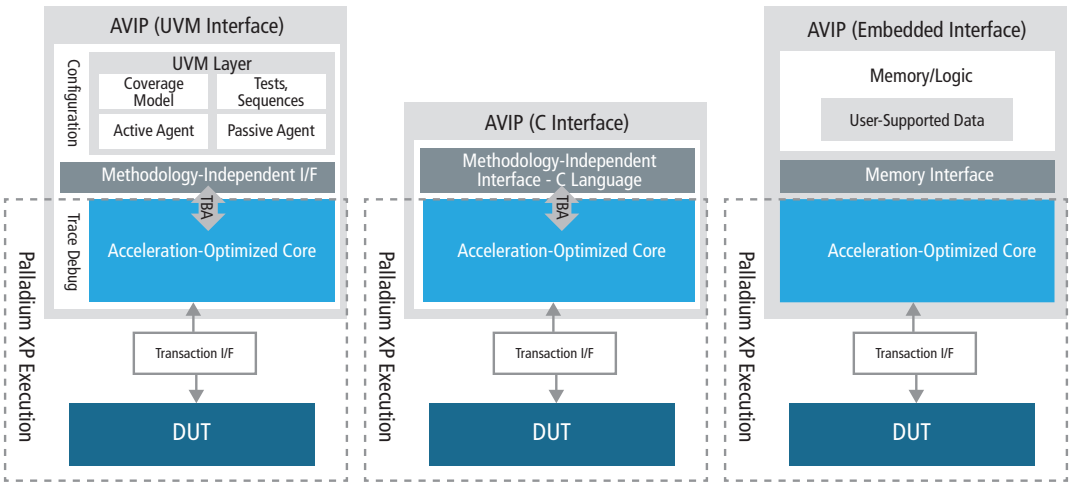

Figure 4: AVIP architecture per interface

To enable UVM reusability, the UVM user interface is leveraged with an optimized core for acceleration. To provide the level of performance required for system-level validation and hardware/software co-verification, an internal transaction-based acceleration interface is included to communicate between the simulator and Palladium XP. The signal interface to the DUT remains, only now it is connected to the optimized core for acceleration.

This implementation enables Cadence AVIP to run the majority of simulation sequence and constraint definitions utilized by protocol test suites or defined by users. AVIP provides coverage reported by the UVM user interface. Even greater performance is provided by the C user interface and the embedded use models. The increased performance is achieved by bypassing the UVM verification layers. The implementation of the protocol stack for USB 3.0 and PCI Express AVIP are shown in Figures 5 and 6, respectively.

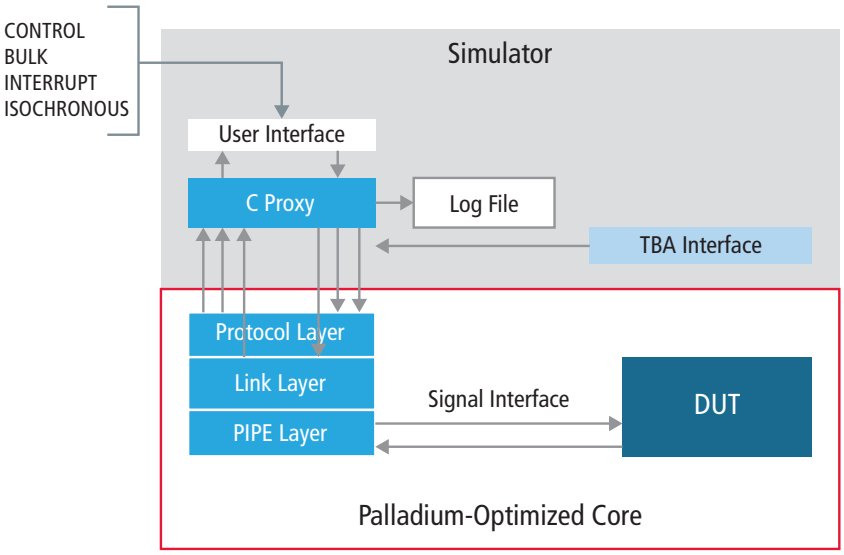

Figure 5: USB 3.0 AVIP

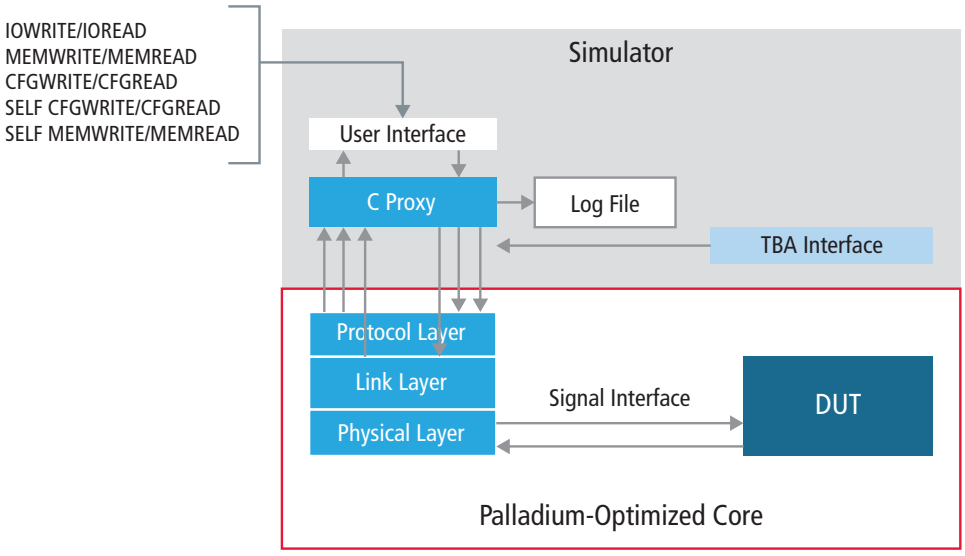

Figure 6: PCI Express 2.0/3.0 AVIP

Creating "Acceleratable" VIP Components

Cadence provides an extension to the standard UVM, enabling users to create Accelerated VIP for their own proprietary protocols. This extension is known as UVM Acceleration, or UVMA. It allows portions of a standard UVM environment to be accelerated using Palladium XP. The same component can be run in both simulation and acceleration since it is compatible with any UVM-based environment.

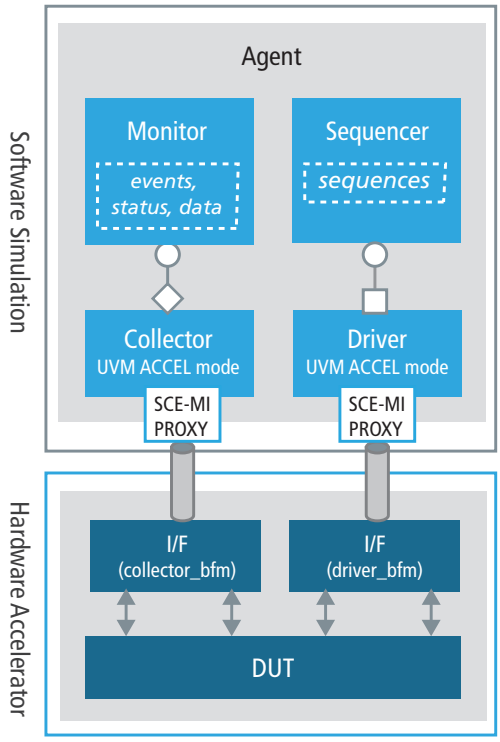

Figure 7: Creating "acceleratable" VIP with UVMA

Cadence UVMA consists of an extension to the UVM library, a methodology, and examples to help UVM simulation users to shorten the time needed to get to acceleration and optimize acceleration performance. The methodology describes how UVM users can build "acceleratable" Universal Verification Components (UVCs) in either SystemVerilog or e language. It describes how the UVC agent can be architected to operate in simulation as well as hardware acceleration. The underlying technology complies with the Accellera Standard Co-Emulation Modeling Interface (SCE-MI) standard. In addition, the methodology is compliant with advanced verification techniques such as metric-driven verification, allowing users to build even greater intelligence into their verification environments. And of course, Cadence AVIP is compatible with UVMA.

Key Capabilities of Simulated VIP and Accelerated VIP

The Cadence VIP portfolio is implemented using a unified architecture, which enables reuse between simulation and acceleration modes for each integration level. VIP is optimized for the underlying platform and use models.

	Simulated VIP (UVM)	Accelerated VIP (UVM)
Performance	• Written as software objects to optimize for high simulation performance	• Acceleration-optimized core for maximum performance in Palladium XP • Performance-optimized memory access • Transaction-based interface for high-speed data transfer
Generation and coverage	• Full-random stimuli model capable of reaching high coverage for all possible combinations • Virtual field for improved access into the core	• Adjustable generation ("knobs"), designed to allow users to optimize tradeoff between verification thoroughness vs. performance
Checking	• UVM layer plus simulation-optimized core • Comprehensive set of checks	• UVM layer plus acceleration-optimized core • SoC-level type checks

Summary

To shorten verification time and increase design quality, Cadence has added Accelerated VIP (AVIP) to its already extensive and industry-leading VIP Catalog. This extended Catalog provides users with the greatest range of verification capabilities to meet their unique verification challenges. Plus, Cadence technology provides users with control over tradeoffs (coverage vs. performance) based on integration level and development phase. To ensure the best performance and verification capability, Cadence VIP provides an optimized core best suited to the type of verification being performed (simulation or acceleration).

Cadence is actively engaging with customers on SoC/system-level verification projects using Accelerated VIP, and is ready to assist you.