

# HDMI 2.0 Design and Verification Challenges

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HDMI designs face challenges with respect to run time and memory consumption due to the huge size of HDMI frames. Scrambling adds more complexity and designs face synchronization and timing challenges. Similar challenges are faced during the functional verification of systems-on-chip (SoCs) including HDMI interfaces. These challenges can be addressed using HDMI verification IP (VIP).

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## Introduction

High-Definition Multimedia Interface (HDMI) is an audio/video (A/V) transmission protocol, which is omnipresent in consumer electronics, personal computing, and mobile products. Modern-day requirements of big screen resolutions, 3D, and multi-channel/multi-stream audio have pushed display devices to use a completely digital, high-speed transmission media, requiring a multi-layered protocol like HDMI.

HDMI 2.0 is the next generation of the popular audio/video high-definition standard and it is the successor to the current HDMI 1.4a/b specifications. The oncoming rise of 4K Ultra HD is the reason behind the entry of HDMI 2.0 into the market. Since 4K Ultra HD is four times the resolution of 1080p, the current HD standard, there is a need for more throughput to handle large amounts of data. Some of the key features of the HDMI 2.0 specification include scrambling, character error detection, and dynamic auto lip-sync.

## Functional Overview

HDMI is a high-speed, serial, digital signaling system that is designed to transmit large amounts of digital data over a long cable length with very high fidelity and reliability. To achieve these goals, HDMI utilizes transition minimized differential signaling (TMDS), which is optimized for robust digital data transmission. HDMI 2.0 incorporates scrambling and TMDS encoding of digital data to reduce electromagnetic interference (EMI) and radio frequency interference (RFI).

Some of the HDMI key features include 4Kx2K frames, TMDS encoding, scrambling, error character detection, BT.2020 colorimetry support, multi-channel audio, 3D audio, multi-stream audio extension, dynamic auto lip-sync, color depth, pixel encoding, HDCP, and 3D/3D dual view.

## 4Kx2K frames (Ultra HD Video)

4Kx2K frame support allows HDMI to transfer extremely high (4X greater than 1080p) video resolutions. Also termed as 4K ultra high definition (HD), 4Kx2K frames support 3840 pixels x 2160 lines as well as 4096 pixels x 2160 lines of video. There are several methods of 4Kx2K frame support:

- Transfer lower 4K x 2K resolution is achieved by cutting the frame rate to 24Hz (less than half of current frame rate of 60Hz) and maintaining the current bandwidth of 340MHz.
- Transfer full 4K x 2K resolution at 60Hz by using 4:2:0 pixel encoding and 4k2k60 8-bit video resolution at 300MHz.
- Transfer full 4K x 2K resolution at 60Hz, at a TMDS clock equal to 600MHz and a data rate equal to 6Gb/s.

## TMDS encoding

TMDS encoding is achieved by the transmitting device by reducing the number of transitions between ones and zeros. While encoding the signal, the transmitting device keeps track of whether and what type of transition reduction or minimization has been done. The receiving device decodes the data using the same mechanism and recreates the original digital signal. TMDS encoding thus ensures proper reception of the signal by clearly demarcating the beginning and end of each byte.

## Scrambling

In HDMI 2.0, scrambling of the digital data is done prior to the TMDS encoding. A linear feedback shift register (LFSR) is set to a pre-defined seed value for each of the three TMDS channels. The digital data is then scrambled using specific bits of the LFSR for the respective channel. Each of the three LFSRs is then incremented to its next state. This process is repeated for every character/pixel being transmitted and is periodically reset once per frame.

## Character error detection

Character error detection provides a mechanism for the receiver devices (e.g., SINK) to report the number of character errors detected. It maintains "error counters" to store number of character errors detected for each channel. A transmitting device periodically samples the error counters to sense the link quality and make adjustments to the outbound data so as to keep the link error to a minimum.

## BT.2020 colorimetry support

The specification proposes optional supports for ITU-R BT.2020 for pixel encodings with 10 or more bits per color component.

## Multi-channel audio

The 22.2 multi-channel audio ensures extremely good sound quality and generates sound impressions with much closer natural sound than 5.1, 6.1, and 7.1 multi-channel audio formats, which are used in current digital sound broadcast. Primary channels for 5.1, 6.1, and 7.1 audio formats lie in the middle layer, while the 22.2 multi-channel audio format allocates channels in front of, to the sides, and in back of the listener. This allows motion of sound images in forward and backward directions.

## 3D audio

The specification proposes an audio system where speakers can be placed anywhere in 3D space. 3D audio uses the channel layouts defined in ITU-R BS.2159-4 (Type B 10.2ch), SMPTE 2036-2 (22.2ch), and IEC 62574 (30.2ch). 3D audio also includes the down-mixed audio streams defined in these standards, provided that the down-mixed audio stream includes nine or more audio channels.

## Multi-stream audio extension

This specification defines a mechanism to concurrently transmit two, three, or four audio streams with the same sample-per-frame rate when supporting multi-view video streaming (e.g., dual-view gaming with different audio for each view) or single-view video streaming (e.g., multilingual support).

## Dynamic auto lip-sync

A dynamic auto lip-sync (DALSS) feature enables synchronization of audio and video in receiver devices that are capable of dynamically modifying their latency. Receiver devices (SINK) declare their latency information for audio and video in the extended display identification data (EDID) field. Transmitting devices (SOURCE) choose the best synchronization mechanism for rendered audio and video data based on the EDID latency field. The HDMI 2.0 DALSS feature allows SINK devices to announce their latency information at any point in transmission so that the SOURCE devices are aware of the correct latency.

## Color depth

Most of today's consumer electronics devices support rich color capabilities and require a greater precision of color depth to avoid artifacts such as banding and contouring. HDMI supports deep color modes of 24 bits, 30 bits, 36 bits, and 48 bits. Deep color mode allocation essentially means better picture quality with a large number of shades of colors.

## Pixel encoding

To support the pixel encoding requirements employed by most current-generation consumer electronics devices, HDMI supports pixel encodings of type RGB 4:4:4, YCbCr 4:4:4, and YCbCr 4:2:2. In addition to the existing HDMI1.4 pixel-encoding types, HDMI 2.0 also supports YCbCr 4:2:0 pixel encoding.

## HDCP

High-bandwidth Digital Content Protection (HDCP) is an encryption mechanism that is used for protection of digital data across the transmitting and receiving devices. The process of authentication and key exchange makes sure that the receiver is authorized to receive digitally protected content.

## 3D/3D dual view

3D video format support was introduced in HDMI1.4b. 3D video formats carry twice as many video pixels at twice the frequency of a 2D video frame. HDMI supports both progressive and interlaced formats with different layouts like frame packing, top and bottom (over/under), side-by-side, half/full, etc.

In addition to 3D video formats, HDMI 2.0 supports 3D dual view. 3D dual view signaling combines two 2D video signals of the same video format type in a single 3D video format.

## HDMI Block Diagram

Figure 1 shows a block diagram of an HDMI transmitter (SOURCE) and a receiving device (SINK) with high-level functional building blocks.

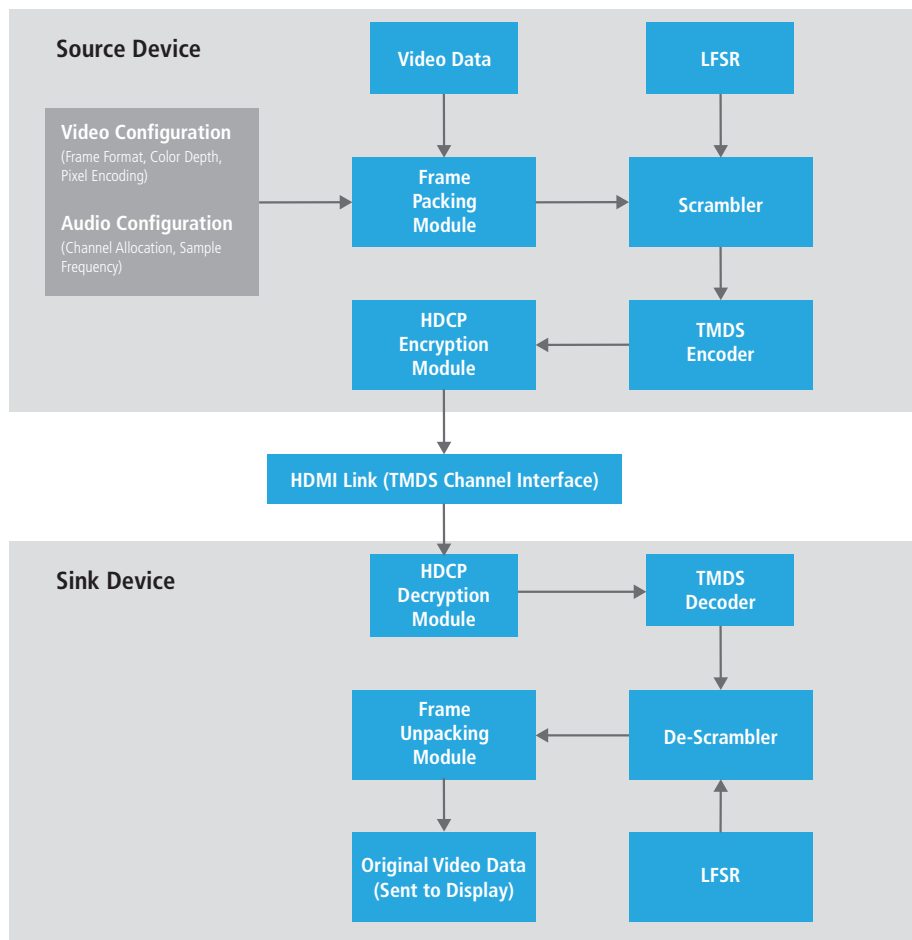


Figure 1: Block diagram of an HDMI transmitter (SOURCE) and a receiving device (SINK)

## HDMI 2.0 Design Challenges

HDMI 2.0 has several features that pose different design challenges, including a redesign of the DUT blocks and changes to the state machine.

A re-design of the blocks within the DUT posed the following issues:

- A legacy video encoder originally synthesized at 300MHz (HDMI1.4b) needed to be synthesized at 600MHz (HDMI2.0) to support new functionality. The combinational path needed a re-design to achieve timing closure at 600MHz.
- Dense combinational logic blocks needed to be pipelined, including an impacted path from the video input stage to TMDS encoder block.
- Due to new timing constraints, several blocks need to be re-designed or re-timed, plus misalignment of control logic between the video sink and video data.
- Sink VIP helped validate the frequency requirement, providing the ability to track the expected output.

The state machine was extended and changed to support the following features:

- New state “scrambling\_enb” in legacy-design state machine to support scrambling for EMI/RFI reduction at TMDS bit rate of lesser than or greater than 3.4Gb/s.
- Dynamic nature of 8-bit unscrambled control period and LFSR functionality.
- Scrambling using the linear feedback shift register (LFSR). The LFSR state advances by eight cycles per TMDS character, adding more complexity to the 600MHz design. The LFSR logic in the source DUT was verified effectively by validating the data decoded by the sink VIP on all the three channels.
- At the source side, all video data and data islands are scrambled.
- On the sink side (VIP), scrambled video pixels and data islands are extracted, decoded, and unscrambled correctly without losing the LFSR synchronization.
- To support CTS testing feature, specification proposes to send SSCP every one or more horizontal lines.
- VIP also supports complex CTS testing requirements laid down by the HDMI2.0 specification:
  - Capable of handling one SSCP per one or more horizontal lines.
  - Re-initialize its LFSRs for all three data channels, whenever it determines that it has received unscrambled control characters simultaneously on all the data channels. This features helps in speeding up the verification of the DUT from the CTS testing perspective.

## HDMI 2.0 Verification Challenges

HDMI protocol verification complexity is increasing exponentially with every protocol iteration from HDMI 1.3x and 1.4x, to 2.0, due to the addition of new frame formats, packet types, encryption, encoding, scrambling, etc. Apart from the protocol complexity, video verification mandates huge video frames, complex data structures with multiple layers, and handling multiple streams, all the time ensuring that there is no loss of data and synchronization between the streams. Encoding, scrambling, and encryption of the digital data makes it even more complex for the VIP to generate and process it at such high speeds.

Development of VIP for such complex protocols is extremely challenging considering that users are looking to minimize test run time and memory consumption impact, and are looking at using different platforms and languages for doing verification at the block, sub-system, and SoC levels.

To make sure that the design is properly verified, all the supported video formats must be checked with all the possible configuration settings, such as frame rate, pixel encoding, color depth, etc. In addition, verification of the design should cover all audio formats supported with appropriate configuration settings (channel allocation, audio sample frequency, etc.).

## HDMI 2.0 Verification IP

Silicon design houses are constantly looking to reduce the time to market for their products. Extremely aggressive timelines and limited resource allocation requires them to have highly adaptable test and verification environments for their SoCs. This essentially means plug-and-play verification components, which are generic in design and configurable for different environments (e.g., platforms, languages, capabilities, etc.).

To cater to the requirements of a vast majority of silicon design houses, a highly flexible, scalable, and proven VIP development methodology is adopted. The methodology is carefully architected so that the developers have enough flexibility to add desired VIP-specific capabilities (e.g., protocol checkers, scoreboards or data checkers), and at the same time keep watch on the memory footprint and CPU run times.

To be able to thoroughly verify the DUT, the VIP must be robust and at the same time provide enough flexibility and configurability to the user, so as to cover both the typical and corner-case scenarios. Some of the features for HDMI VIP include:

- Static configuration parameters—Constant across different set of frames (e.g., SOURCE/SINK device type, physical addresses).
- Dynamic configuration parameters—May change across frames (e.g., video format, color depth, scrambling enable/disable).

- Customizable frame formats—Due to the huge frame sizes (hence large run times), there has been a growing demand for customizable frame formats to be supported by VIP. Custom frame sizes help users to verify the basic functionality using smaller frames in less simulation cycles. HDMI VIP supports non-standard frame formats to enable users to run simulations with smaller frames.
- User-controllable options—Provides a robust and wide range of user-controllable options without sacrificing the run time performance and memory consumption.
- Configuration-level, packet-level, and field-level error-injection capabilities.
- Frame boundary detection—For both 2D as well as 3D frames by the receiver VIP.
- Detection and automatic switching—Between scrambled and unscrambled modes by receiver VIP while maintaining LFSR synchronization across frames.
- On-the-fly data-integrity and signal-integrity checkers, as well as compliance test suite (CTS) checkers—VIP allows the creation of different CTS test scenarios for all mandatory protocol features (frame formats, audio formats, etc.) as defined by the HDMI specification.
- 100% coverage—Most of the VIP users rely on the coverage being reported by the VIP. Cover points for a wide range of test scenarios are supported to achieve 100% coverage with respect to the user's verification plan.

Figure 2 shows a testbench configuration with the VIP configured as a source connected with a sink DUT.

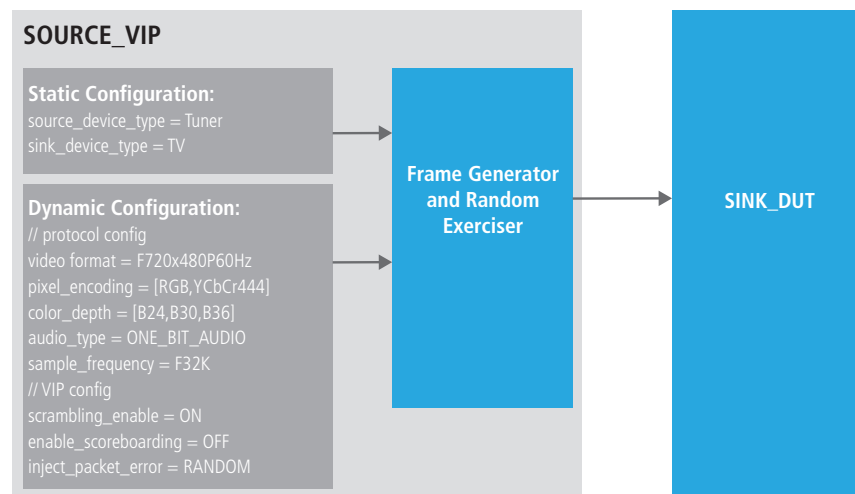


Figure 2. VIP configured as HDMI source for sink DUT

## Conclusion

HDMI designs face challenges with respect to run time and memory consumption due to the huge size of HDMI frames. Scrambling adds more complexity and designs face synchronization and timing challenges. Similar challenges are faced during the HDMI verification. These challenges can be addressed using HDMI VIP with the following capabilities:

- Non-standard features that allow the verification of a large number of scenarios with less simulation time and memory consumption.
- Layered and scalable architecture of HDMI VIP provides a smooth and timely migration from the IP-level verification environment to the SoC-level verification environment.
- Reusability of tests across simulation and acceleration environments.
- Use of HDMI VIP to reduce the overall verification effort.

### Further Information

1. Speed Design of Ultra HD Displays with Cadence HDMI 2.0 Verification IP:  
[www.cadence.com/cadence/newsroom/features/Pages/HDMI2\\_0.aspx](http://www.cadence.com/cadence/newsroom/features/Pages/HDMI2_0.aspx)
2. HDMI Forum—HDMI 2.0 Overview:  
[www.hdmi.org/manufacturer/hdmi\\_2\\_0/index.aspx](http://www.hdmi.org/manufacturer/hdmi_2_0/index.aspx)



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