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Tensilica Datasheet

Cadence Tensilica ConnX BBE32EP Enhanced Performance DSP Core for Baseband Processing

Configurable, Extensible, Scalable

The Cadence® Tensilica® ConnX BBE32EP enhanced performance digital signal processor (DSP) core establishes a new standard in high-performance, low-power digital signal processors specifically designed for high-performance baseband processing. Optimized for complex number processing, the Tensilica ConnX BBE32EP core offers significant improvements in maximum frequency and algorithmic performance while reducing both silicon area and power consumption versus earlier generations of DSPs. The ConnX BBE32EP is the first DSP truly suitable for inclusion in both infrastructure and user equipment applications. Easily optimized through check box options, the Tensilica ConnX BBE32EP along with the larger Cadence Tensilica ConnX BBE64EP provides unprecedented flexibility in implementing systems at power consumption levels that significantly reduce the need for hardware accelerators.

Features

- 32-way multiplier-accumulator (MAC), dual 16-way arithmetic logic unit (ALU) single instruction, multiple data (SIMD) engines
- 5-issue very long instruction word (VLIW) for parallel load/store, MAC, and ALU ops
- 32-bit scalar ALU
- Advanced Precision for matrix inversion and divide operations
- Optimized instructions for:
  - Complex arithmetic
  - Polynomial evaluation
  - Matrix multiplication
  - Block floating point
  - Bit-oriented operations
  - Vector compression and expansion
- Predicated vector instructions
- Wide memory bandwidth
  - 256-bit load/store and 256-bit load units
- 10-stage DSP pipeline
- High-performance C/C++ compiler with automatic vectorization of scalar C and full support for vector data
- TI intrinsic support; rich application libraries

Benefits

- High performance, low power over a broad range of algorithms including support for LTE Advanced, LTE, HSPA+, and Wi-Fi including multiple-input and multiple-output (MIMO)
- Fast baseband development through familiar C programming with general-purpose digital signal processing and 2G/3G/4G/Wi-Fi specific library support
- Full support for hardware/software co-design
- Easy integration into system SoC simulations with functional, cycle-accurate, and hardware pin-level models
- **Configurable** instruction set with 12 predefined, pre-verified vector packages, from fast Fourier transforms (FFTs) to Advanced Precision arithmetic
- **Extensible** instruction set support through the TIE language
- **Scalable** with customized FIFO, port, and lookup interfaces

High Performance, Maximum Flexibility

Fast time to market, evolving standards, and long platform lives are all incompatible with the rigidity of ASIC-based designs. Whether it's a microcell, an access point, a mobile hotspot, a tablet, or a set-top box, all can benefit from the flexibility of a software-based solution. This flexibility can only be achieved by the use of modems that implement the signal processing on programmable processors.

The ConnX BBE32EP is built on Cadence's proven Tensilica Xtensa® LX customizable processor architecture and is specifically designed to support the needs of baseband signal processing. It delivers the processing capacity needed in multi-user systems and has a broad instruction set specifically targeted at 3G, 4G, and Wi-Fi systems. This allows you to minimize hardware accelerators in the processing chain, making the system not only more flexible, but also lower risk.

Beyond simple software programmability, support for push-button assembly of optimized processors is at the heart of all Xtensa-based ConnX products. This includes the ability to:

- Integrate targeted pre-built, verified function blocks
- Add/subtract from the basic instruction set

- Add full custom instructions through hardware (including full C programming support)
- Integrate the ConnX BBE32EP core into complex systems through a variety of general-purpose and performance-optimized interfaces.

Whether implemented as a single core, as an array of ConnX BBE cores or a hybrid system on chip (SoC) made up of a diverse mix of ConnX processors and hardware accelerator blocks, the ConnX BBE32EP core is there to do the heavy lifting at the intersection of maximum performance and flexibility.

Configurable, Extensible, Scalable

The ConnX BBE32EP core provides 12 pre-built vector options. These options are included/excluded as checkboxes when defining a core and result in seamless integration of a feature into the hardware, the compiler, the modeling tools, and the verification scripts. With these capabilities, you can build a custom core without the large development schedule impact that a change in hardware design would normally involve.

The ConnX BBE32EP core can be extended to support custom ports and queues for efficient connection to offload accelerators and are fully supported in programming and modeling tools. These custom interfaces can be defined to match the interfaces of existing third-party intellectual property (IP). Thus, the ConnX BBE32EP core can access hardware offload accelerators in a single cycle deterministic operation, greatly reducing power consumption and without impacting the shared system bus.

Application Space: LTE-A, LTE, WCDMA, Wi-Fi

The ConnX BBE32EP baseband engine is a high-performance DSP designed for next-generation communication systems such as LTE Advanced, LTE, WCDMA, HSPA+, WiFi and DVB. Advanced Precision options are specifically designed to meet the precision and performance requirements associated with advanced MIMO systems. In addition to vector-based filtering, FFT, and matrix capabilities, a fully featured instruction set includes a full range of bit-oriented operations. As such, the ConnX BBE32EP processor excels at multi-standard physical layer processing, providing opportunities for hardware savings and a broader scope of applications than a dedicated fixed hardware solution could provide.

As physical layer (PHY) system developers move to advanced standards such as LTE Advanced, they face the need for dramatic increases in performance from their processing platforms. The ConnX BBE32EP core meets this challenge with its highly parallel vector engines and with an architecture identical to that of the ConnX BBE64EP, providing an easy upgrade path when needed. When processing needs scale beyond that of a single DSP, the ConnX BBE32EP/64 family provides smooth support for multi-core solutions.

As systems become more diverse with wide-scale deployment of heterogeneous networks, the solution that may work best for a microcell operating on a bullet train in Japan may be very different from a similar microcell operating in a subterranean pedestrian mall in downtown Montreal. A programmable software-based solution using the ConnX BBE32EP core allows you to implement both solutions on a single platform, permitting it to evolve without going back for a re-spin of silicon.

With a solution based on the ConnX BBE32EP core, you can deliver a working solution in less time than a traditional hardware or a hybrid hardware/DSP design. You can also take advantage of the hardware platform for a broader range of applications, over a longer period of time. Ultimately, this reduces costs and results in faster time to market, helping you deliver more competitive solutions in the marketplace.

Toolchain

The ConnX BBE32EP processor is delivered with a complete set of software tools. The toolset includes a high-performance C/C++ compiler with automatic vectorization to support the VLIW pipeline in the core. This comprehensive toolset also includes the linker, assembler, debugger, profiler, and graphical visualization.

A comprehensive instruction set simulator (ISS) allows you to quickly simulate and evaluate performance. When working with large systems or lengthy test vectors, the fast, functional TurboXim™ simulator option achieves speeds that are 40X to 80X faster than the ISS for efficient software development and functional verification.

System C (XTSC) and C-based (XTMP) system modeling can aid in full-chip simulations. Pin-level XTSC offers co-simulation of SystemC and RTL level offload accelerator blocks for fast, cycle-accurate simulations.

The core supports all major back-end EDA flows, and represents the next generation in push-button customizable DSP cores from Cadence, the leader in configurable, extensible, and scalable solutions for advanced communications systems. Its proven development environment for both hardware and software reduces time to market and risk, and provides maximum flexibility in baseband processing solutions for 4G, 3G, Wi-Fi, and beyond.

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